Intel-Based Electronic Classroom Student Computing Station Based on the Intel® Celeron™ Processor and Intel® 810 Chipset

Reference Configuration

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Order Number: 273292-002

Application Note

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1.0 Introduction

1.1 Purpose

This application note describes how Intel® architecture processors, chipsets, and other components can be used in designs for Intel-based electronic classroom student computing stations. An Intel-based electronic classroom is an educational setting in which a network of computers is used as a primary teaching, learning, and assessment tool. A typical Intel-based electronic classroom contains an instructor's system that broadcasts application software to, and often receives data from, student computing stations. The student computing stations can be configured and administered at the server level.

Intel architecture components are well-suited for Intel-based electronic classroom systems. Using PC-based building blocks in these designs provides flexibility, upgradability, ease of administration, and high performance for graphic-intensive and internet applications. In addition, Intel architecture processors are compatible with a wide variety of operating system and off-the-shelf application software. This application note describes a typical Intel-based electronic classroom network and provides a reference design for Intel architecture-based electronic classroom student computing stations.

Schematics for the reference design are provided in Appendix B of this document.

1.2 Terminology

The following terms are used in this document.

Term	Definition
Intel-Based Electronic Classroom	An electronic teaching and learning environment that uses dedicated, connected student computing stations to implement a specific educational curriculum
Remote boot	A client operating system boot up from a server in a network environment
TCO	Total cost of ownership
ISV	Independent software vendor
WfM	Intel's Wired for Management initiative

1.3 Revision History

Revision	Date	Notes
001	October 15, 1999	Initial version.

2.0 Intel-Based Electronic Classroom Environment Overview

An Intel-based electronic classroom is a teaching and learning environment that uses a server-client system in the classroom to implement the curriculum. Teaching and learning is done using a teacher station, student computing stations, and specific educational software applications and content. With this modern educational technology, educators can deliver intuitive online courses, training, demonstrations, and examinations. They can also incorporate access to the Internet and intranet to enrich the educational experience.

An Intel-based electronic classroom LAN environment can consist of up to 60 student computing stations, a teacher station, and a network server. In an Intel-based electronic classroom, every student computing station is administered centrally. These student computing stations have high reliability and security, and low maintenance costs. The student computing stations have a subset of a PC feature set: they typically have a different motherboard configuration (described in Section 4.0) and are configured without a CD-ROM drive or hard disk. This solution provides a greater access to the necessary technology while simplifying maintenance and reducing the total cost of ownership.

In schools, PCs can be used in teacher offices as productivity tools for administration and development of teaching materials. These materials may then be used in Intel-based electronic classrooms to teach subjects such as computer skills, languages, sciences, and mathematics. The teacher uses the teacher station in the Intel-based electronic classroom to guide students through the lesson, while each student follows the lesson on his/her own student computing station. The students can also use their student computing stations independently to practice lesson materials and learn other application software.

Desirable features of Intel-based electronic classroom student computing stations include the following:

- Ease of management and maintenance

  Primary and secondary schools typically do not have a full time Information Technology (IT) staff to manage the Intel-based electronic classroom. Most IT administration is done by teachers and student volunteers. Hence, the student computing stations used in the Intel-based electronic classroom must be easy to manage.

  Intel-based electronic classroom student computing stations can be configured without CD-ROM and floppy drives. This further simplifies the management of these student computing stations by preventing students from erasing files or corrupting the operating system and applications.

- Low total cost of ownership (TCO)

  Schools have limited budgets for setting up Intel-based electronic classrooms. Therefore, a key consideration is affordability in terms of initial capital and ongoing maintenance costs, including the costs of off-the-shelf educational applications and teaching content.

- Software availability and compatibility

  Establishing a productive Intel-based electronic classroom depends on the availability of system-compatible, off-the-shelf applications and teaching materials. It is important that schools have tools to develop customized content to meet the particular needs of their students.

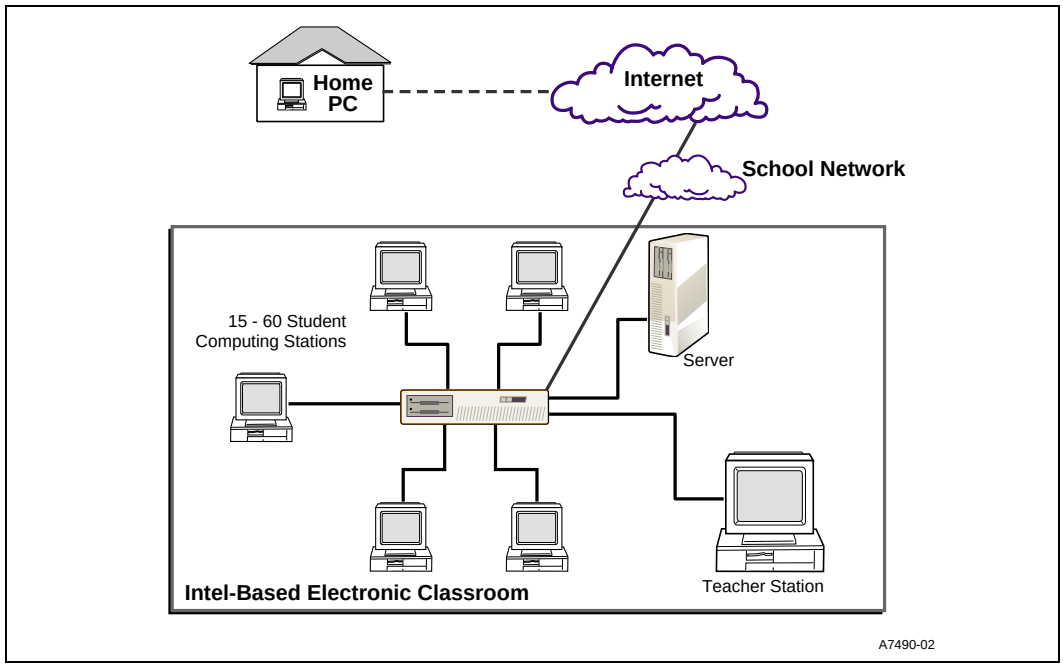
- Product life cycle support

  Schools use Intel-based electronic classroom student computing stations for several years before considering an upgrade. Therefore, replacement parts should be available for this duration.

3.0 Intel-Based Electronic Classroom Setup and Operating Environment

A typical Intel-based electronic classroom setup is depicted in Figure 1.

Figure 1. Typical Intel-Based Electronic Classroom Setup



The student and teacher stations are linked together in a LAN environment via a network hub or switch device. The LAN network enables the remote boot for diskless student computing stations and file sharing among all the student computing stations. The broadcasting capability is implemented through software using the existing LAN infrastructure. This solution reduces overall system cost, simplifies wiring and upgrade requirements, and enables the use of higher performance processors.

The components of a typical Intel-based electronic classroom and their recommended configuration are described in Table 1.

Table 1. Intel-Based Electronic Classroom Hardware Descriptions and Recommended Configuration

Item	Quantity (units)	Recommended Configuration
Teacher Station	1	Intel® Pentium® III processor, 64 -128 Mbyte SDRAM, Intel® 440BX AGPset, Hard-disk, Intel® Network Card, Video Capture Card
Student Computing Station	15 - 60	Intel® Celeron™ processor 433 MHz or better (in 370-pin PPGA) and Intel® 810 chipset, 32 Mbyte SDRAM, Intel Network Card integrated on board, Hard-disk (optional)
Server	1	Pentium III processor, 128 Mbyte SDRAM, Intel® L440GX motherboard, SCSI Hard-disk, Intel Network Card
Switch	1-3	Intel Express 510T, 24 10/100Mbit Switching Port
Router	1	Intel Express 9500 Router for Internet connection
Multimedia teaching Software	1	From ISVs. Based on TCP/IP or IPX network protocol. Intel® LANSchool software site is a basic reference: http://www.intel.com/network/products/lanschool.htm

3.1 Intel-Based Electronic Classroom Configuration

The configuration of the Intel-based electronic classroom depends on the size of the classroom, the network design, and the use of the multimedia broadcasting software. The following describes an example configuration that consists of five main parts:

- Network environment
- Teacher Station management system
- Multimedia broadcasting software
- Application and education software
- Intel-based electronic classroom student computing stations that remote boot from server

The following sections describe each component of the example Intel-based electronic classroom.

3.1.1 Network Environment

The network can be set-up using Windows* NT 4.0 or Novell Netware* on the server. The teacher station and student computing stations run on Windows 95/98 operating systems. The Intel-based electronic classroom student computing stations boot up remotely from a server that is connected in a LAN environment.

3.1.2 Teacher Station Management System

The teacher station in this example can perform the following functions:

- Broadcasting the teacher station screen

  All teaching materials, including presentation, animations, and movies can be broadcast to the student computing stations.

- Controlling student computing stations remotely

  The teacher can control, reset, and lock the student computing stations or receive the display from a particular Intel-based electronic classroom student computing station.

- Providing online help

  The teacher can provide help through the network when students have difficulty with their assignment. The students would also be able to request assistance through the network.

3.1.3 Multimedia Teaching Software

The multimedia teaching software utilizes a standard LAN network interface through TCP/IP protocol and typically offers the following features:

- Screen broadcasting
  - — Each computing station (teacher's and student's) can broadcast its screen to some or all students. Only one screen can be broadcast at a time.
  - — The teacher can lock each student's keyboard and mouse and can broadcast any student's screen to the class.
  - — All graphics formats, such as MPEG and VCD can be broadcast in real time.
- Audio/voice communication
  - — The teacher's voice can be broadcast to one, several, or all students.
  - — Conferencing is supported in teacher-student, student-student, or other combinations.
  - — The voice can be input through MIC or Line In on the sound card.
- Remote access
  - — The teacher can view any student's screen remotely.
- Grouping
  - — Student computing stations can be grouped in any combination for discussion (screen/audio).
- Question
  - — Students can submit questions through MIC or keyboard (using a special function key).
  - — Two way or multi-way online questioning is supported, as in a "chat" mode.
- Remote reset
  - — The teacher can reset any or all Intel-based electronic classroom student computing stations if an error occurs in the system.
- Examinations can be administered and completed online.

3.1.4 Application Software

Typically, application software, such as word processing and spreadsheet programs, and instructor-developed materials are taught in Intel-based electronic classrooms. In some Intel-based electronic classrooms, students are assessed using on-line examinations.

3.1.5 Remote Booting Intel-Based Electronic Classroom Student Computing Stations from Server

During the remote boot process, the Intel-based electronic classroom student computing stations contact the server (using Preboot Execution Environment in the boot ROM of the network interface), install a boot image, and boot the operating system that is pre-configured on the server. Various operating systems can be remote booted from the server, including Windows 95/98 or Linux*.

The setup is optimized through the availability of the Preboot Execution Environment (PXE) compliant boot ROM. PXE allows the server to set up each student computing station with a specific IP address using the Dynamic Host Communication Protocol (DHCP). The boot ROM then downloads the boot image from the server using the Trivial File Transfer (TFT) protocol. This boot image program then configures the student computing stations and boots the pre-configured operating system. If the Intel-based electronic classroom student computing station's operating system or applications are damaged, they can be recovered by downloading the new image from server when the system restarts. This reduces the total cost of maintenance. Refer to section Section 5.7.2.2, "Remote Service Boot" on page 22 for more information.

4.0 Recommended Motherboard Configuration for Intel-Based Electronic Classroom Student Computing Stations

The motherboard of this reference design for Intel-based electronic classroom student computing stations is a highly integrated design that incorporates many features on the board. It is recommended that system designers use an LPX form factor or Flex ATX design. The LPX form factor enables the student computing stations to have a very slim casing, which is desirable for small Intel-based electronic classroom environments. Flex ATX helps reduce board size and cost. The components listed below provide an example of a motherboard design based on the Celeron processor and Intel 810 chipset.

Main Components of Reference Motherboard for the Intel-Based Electronic Classroom Student Computing Station:

- Intel® Celeron™ processor 300A/366/433 MHz in 370-pin PPGA
- Intel® 810 Chipset
- Two DIMM sockets that support up to 512 Mbyte (128 Mbit technology) SDRAM
- Two IDE interfaces
- One floppy disk interface
- COM 1 and COM 2 serials ports and a parallel port
- PS/2 mouse and keyboard connectors
- Intel® Flash BIOS
- Super I/O* and USB ports
- 1 X PCI 2.2-compliant PCI slot

Peripherals on Intel-Based Electronic Classroom Student Computing Station:

Integrated audio in chipset

- Audio Codec ’97 2.1 extensions compliant
- Stereo line level output
- One audio out, audio in, and MIC jack

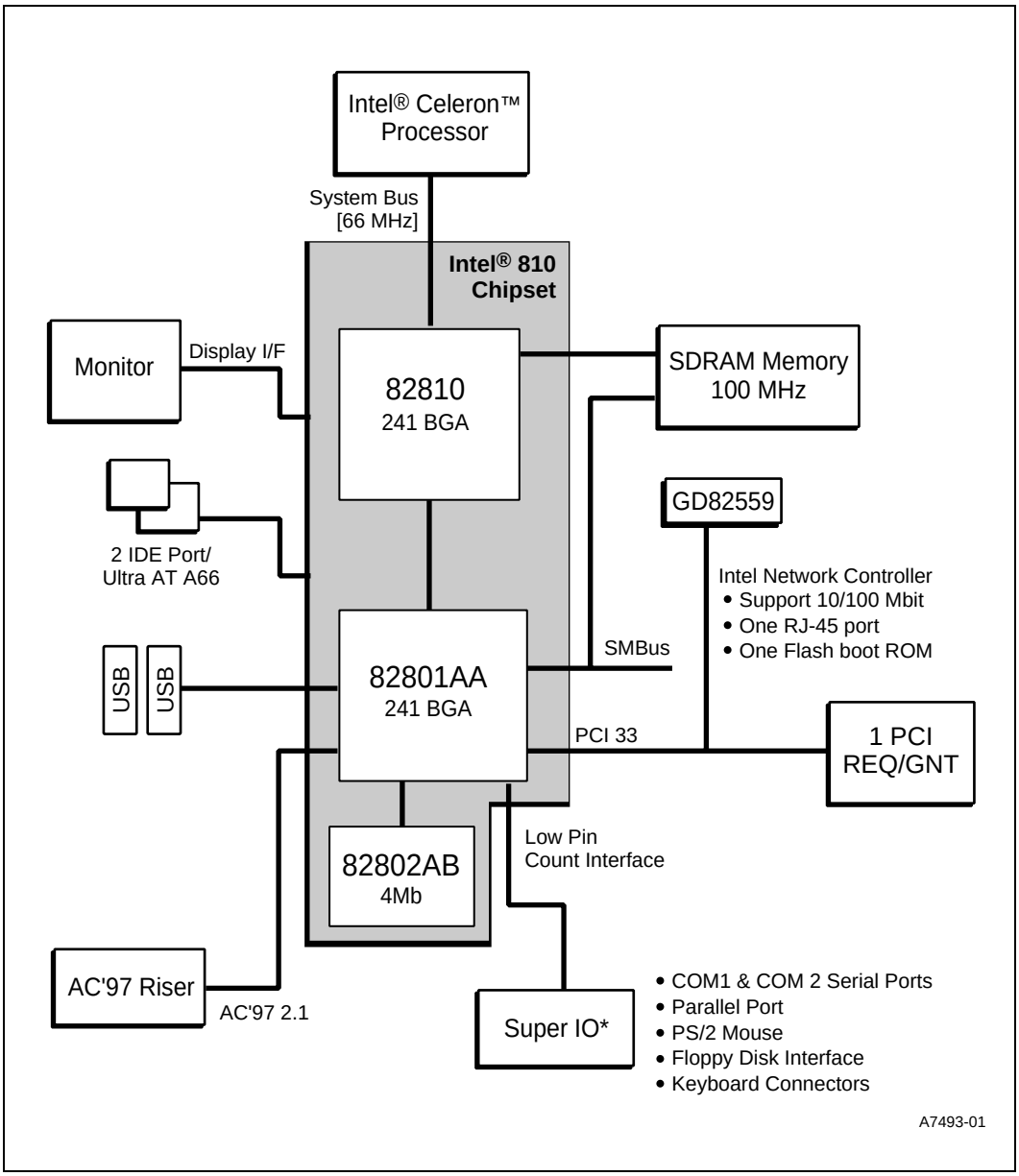
Integrated Graphics

- 3-D graphics with texturing and visual enhancements up to 1024x768x16 @85 Hz refresh
- 2-D graphics up to 1600x1200x8 @85 Hz refresh
- RGB output

PCI-based 10/100 Mbps Network card

- Intel® 82559-based card recommended
- One RJ-45 port
- Boot ROM which contains Intel® Preboot Execution Environment (PXE)

Figure 2. Building Block of the Intel-Based Electronic Classroom Student Computing Station Motherboard



5.0 Design Consideration of Intel-Based Electronic Classroom Student Computing Station Hardware

5.1 Intel® Celeron™ Processor

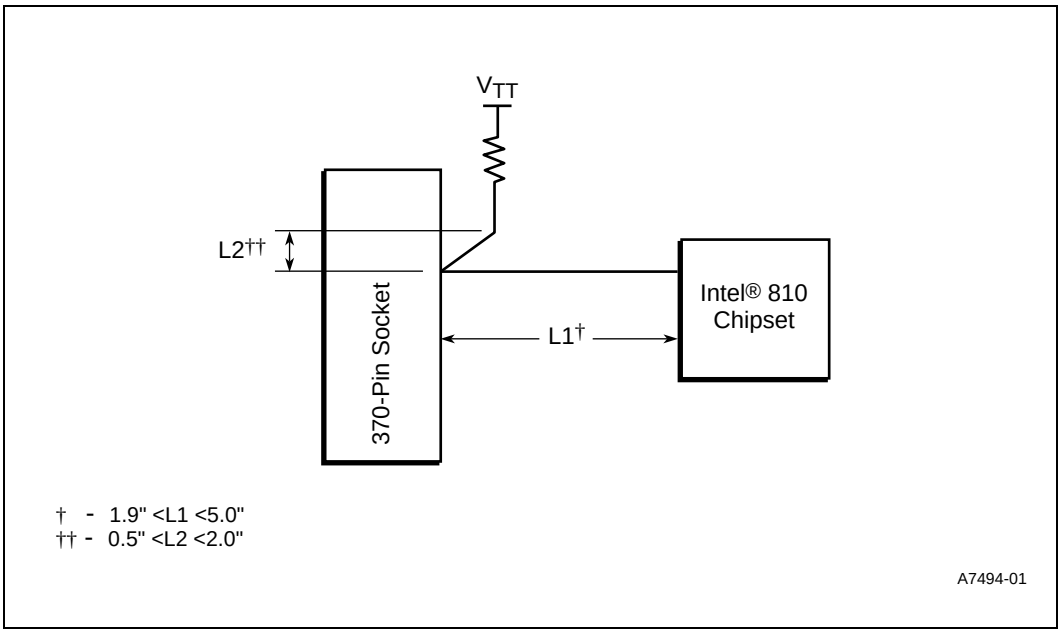
This reference configuration supports the Intel Celeron processor at 300, 366 MHz and 433 MHz in a Plastic Pin Grid Array (PPGA) package.

The Intel Celeron processor PPGA package implements a Dynamic Execution micro-architecture and executes MMX™ media technology instructions for enhanced media and communication performance. The Intel Celeron processor PPGA is based on the P6 family processor core and is provided in a PPGA package for use in low cost systems in the value PC and Intel-based electronic classroom student computing station market segments. The Intel Celeron processor PPGA utilizes the AGTL+ system bus used by the Pentium® II processor with support limited to single-processor systems. The Intel Celeron processor PPGA includes an integrated 128 Kbyte second level cache with separate 16 Kbyte instruction and 16 Kbyte data level-one caches. The second level cache is capable of caching 4 Gbytes of system memory.

5.1.1 Design Notes for the Intel® Celeron™ Processor

The schematics use a Single Ended Termination (SET) network topology in which the termination resistors are located at only the PPGA (processor) side to reduce the system cost, solution space, and ringing effect. In the SET topology, the termination should be placed close to the processor either on the motherboard or on the processor substrate. No termination is present at the chipset end of the network.

Figure 3. Topology for Single Processor Designs with Single End Termination (SET)



5.2 Intel® 810 Chipset

Intel has developed technology that enhances the performance and value of Intel Celeron processor-powered systems. Built on the strong foundation of Intel 440BX AGPset technology, the Intel 810 chipset provides next generation features and great graphics performance at a lower cost.

The Intel 810 chipset contains three core components:

1. Host Controller — Graphics and Memory Controller Hub (GMCH0)

   The GMCH0 (82810) provides the interconnect between the SDRAM and the rest of the system logic:

   — 421 Mini BGA

   — Integrated Graphics controller

   — 230 MHz RAMDAC

   — Support for Intel Celeron processors with a 66 MHz system bus.

   — 100 MHz SDRAM interface supporting 64/256/512 Mbyte with 16/64/128 Mbit SDRAM technology

   — Downstream hub interface for access to the ICH

2. I/O Controller Hub — 82810AA (ICH)

   The I/O Controller Hub provides the I/O subsystem with access to the rest of the system:

   — 421 Mini BGA

   — Upstream hub interface for access to the GMCH0

   — PCI 2.2-compliant interface (6 PCI Req/Grant Pairs for 82801AA ICH)

   — Bus Master IDE controller; supports either Ultra ATA/33 or Ultra ATA/66 (82801AA)

   — USB controller

   — SMBus controller

   — FWH interface

   — LPC interface

   — AC’97 2.1 interface

   — Integrated System Management Controller

   — Alert-on-LAN (82801AA ICH only)

   — Interrupt controller

3. 82802 Firmware Hub (FWH)

   The 82802 FWH component is a key element to enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include:

   — An integrated hardware Random Number Generator (RNG)

   — Register-based locking

   — Hardware-based locking

   — 5 GPIs

5.2.1 The Intel® 82810 Graphics Memory Controller Hub (GMCH0)

The Intel 810 chipset provides a rich and robust 2-D and 3-D graphics using an integrated chipset design that utilizes second-generation graphics technology. At the core of the 810 chipset is a memory controller with built-in graphics technology. The Intel 810 chip optimizes system memory arbitration, similar to AGP technology, resulting in a more responsive and cost-effective system.

The 82810 Graphics Memory Controller Hub (GMCH0) features Intel graphics technology and software drivers and uses Direct AGP (integrated AGP) to create vivid 2-D and 3-D effects and images. The 82810 chip features integrated Hardware Motion Compensation to improve soft DVD video quality and a digital video out port that enables connection to traditional TVs or the new space-saving digital flat panel displays.

Intel Dynamic Video Memory Technology (DVMT) is an architecture that offers breakthrough performance for the Value PC segment through efficient memory utilization and Direct AGP. The system OS uses the Intel software drivers and intelligent memory arbiter to support richer graphics applications.

The System Manageability Bus allows networking equipment to monitor the 810-chipset platform. Using ACPI specifications, the system manageability function enables low-power sleep mode and conserves energy when the system is idle.

5.2.1.1 Design Notes for the Intel® 82810 GMCH0

The GMCH ball assignment and ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals are routed directly from the GMCH0 to the ICH on the top signal layer. The hub interface has two signal groups:

- Data Signals: HL[10:0]
- Strobe Signals: HL_STB, HL_STB# (differential strobe pair)

There are no pull-ups or pull-downs required on the hub interface.

Hub interface data signals should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH0 and the ICH, the hub interface data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils within 0.3” of the GMCH0/ICH components. The maximum trace length for the hub interface data signals is 7”. These signals should each be matched within ±0.1” of the HL_STB and HL_STB# signals.

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7” and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes with ±0.1”.

HREF is the hub interface reference voltage. It is 0.5 * 1.8 V = 0.9 V ±2%. It can be generated locally, or a single HREF divider can be used. Each divider consists of a DC element and an AC element. The resistors in the DC element should be equal in value and rated at 1% tolerance. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The resistors in the AC element of the resistor divider should be no greater than 80 Ω and the capacitors should be 500 pF. Additionally, the reference voltage should be bypassed to ground at each component with a 0.1 uF capacitor.

5.2.2 The Intel® 82801 I/O Controller Hub (ICH)

The 82801 I/O Controller Hub (ICH) employs the Intel Accelerated Hub Architecture to make a direct connection from the graphics and memory to the integrated AC97 controller, the IDE controllers, dual USB ports, and PCI add-in cards.

The Accelerated Hub Architecture provides twice the bandwidth of the PCI bus at 266 MB per second. This allows a wider flow of rich information from the I/O controller to the memory controller, with optimized arbitration rules allowing more functions to run concurrently, enabling more life-like audio and video.

The Integrated Audio-Codec 97 controller enables software audio and modem by using the processor to run sound and modem software. By reusing existing system resources, this feature adds flexibility, improves sound quality, and lowers the system BOM cost by eliminating components.

The 82802 Firmware Hub (FWH) stores system BIOS and video BIOS, eliminating a redundant nonvolatile memory component. In addition, the 82802 contains a hardware Random Number Generator (RNG). The Intel RNG provides truly random numbers to enable fundamental security building blocks supporting stronger encryption, digital signing, and security protocols.

5.2.2.1 Design Notes for the Intel® 82801 ICH

- **ICH Placement:** The ICH should be placed within 8” of the ATA connector(s). There are no minimum length requirements for this spacing.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- **Series Termination:** There is no need for series termination resistors on the data and control signals since series termination is integrated into these signal lines on the ICH.
- A 1 KΩ pull-up to 5 V is required on PIORDY and SIORDY.
- A 470 Ω pull-down resistor is required on pin 28 of each connector.
- A 5.6 KΩ pull-down resistor is required on PDREQ and SDREQ.
- Support Cable Select (CSEL) is a PC99 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- Primary IDE connector uses IRQ14 and the secondary IDE connector uses IRQ15.
- IRQ14 and IRQ15 each need an 8.2 KΩ pull-up resistor to V_{CC}.
- Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Due to high loading, the PCI_RST# signal should be buffered.
- There is no internal pull up or down on PDD7 or SDD7 of the ICH. Devices should not have a pull-up resistor on DD7. It is recommended that a host have a 10 KΩ pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).
- If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals left as no connects.

5.3 IDE Connectors

The 82801AA ICH supports Ultra ATA/66 and ATA/33 devices The ATA/66 cable is an 80-conductor cable; however the 40-pin connectors used on motherboards for 40-conductor cables do not change as a result of this new cable. The wires in the cable alternate: ground, signal, ground, signal, etc. All the ground wires are tied together at the connectors on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee. To determine if ATA/66 mode can be enabled, the Intel 810 chipset using the ICH requires the system BIOS to attempt to determine the cable type used in the system.

If only one IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals left as no connects. This can be implemented to reduce the board space and cost.

5.4 AC'97 2.1 Compliant Components

The ICH implements an Audio Codec '97 (AC'97) 2.1 compliant digital controller. Any codec attached to the ICH AC-link should also be AC'97 2.1 compliant. Contact your preferred codec vendor for information on AC'97 2.1 compliant products. The AC'97 2.1 specification is available on the Intel web-site:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the following combinations of codecs:

Table 2. AC'97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

The ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

5.4.1 Design Notes for AC'97 Devices

- Special consideration must be given for the ground return paths for the analog signals. If isolated ground planes are used, pin B2 on the AMR connector should be used as an isolated ground pin and should be connected to an isolated ground plane to reduce noise in the analog circuits. The AMR designer and motherboard designer should jointly address any EMI issues when implementing isolated grounds.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in the other.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05" wide.
- Keep digital signal traces, especially the clock, as far way from analog input and voltage reference pins as possible.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (¼" to ½ " wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05"wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground (i.e., there should not be any signals crossing the split/gap between the ground planes). Doing so will cause a ground loop.

5.5 Audio/Modem Riser Card (AMR)

Intel is developing a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options. The AMR specification is available on the Intel developer website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

For the Intel-based electronic classroom student computing station, the audio codec is integrated on the motherboard to avoid compatibility issues and robustness. A modem codec is optional for electronics classroom.

5.5.1 Design Notes for the Audio/Modem Riser Card

- Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
- As the Intel-based electronic classroom student computing station motherboard implements an active primary codec (audio) on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground. The PRI_DN# pin is provided to indicate that a primary codec is present on the motherboard.

5.6 PCI

The ICH provides a PCI bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification*, Revision 2.2. The 82801AA ICH supports 6 PCI bus masters (excluding ICH), by providing 6 REQ#/GNT# pairs. The PCI network controller (GD82559) is integrated on board; therefore, an extra PCI slot is expandable for a PCI network broadcasting card (if implemented).

5.7 Network Controller — Intel® 82559 Fast Ethernet Controller

The 82559 10/100 Mbps Fast Ethernet controller with an integrated 10/100 Mbps physical layer device is Intel's leading solution for PCI board LAN designs. It is designed for use in Network Interface Cards (NICs), PC LAN On Motherboard (LOM) designs, embedded systems, and networking system products. The 82559 combines a low power and small package design which is ideal for power- and space-constrained environments. It is compliant with Advanced Configuration and Power Interface (ACPI) 1.20A-based power management and with the Wired for Management (WfM) 2.0 Baseline specification.

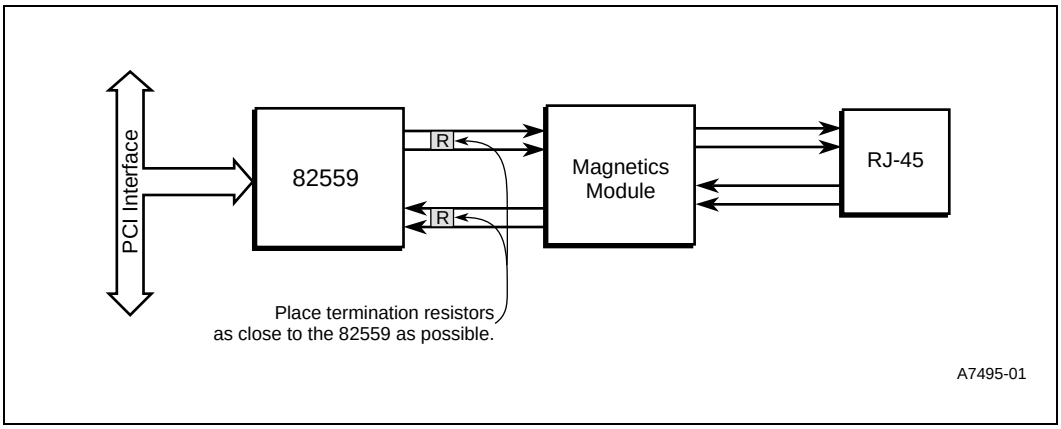
The 82559 is an integrated IEEE 802.3 10BASE-T and 100BASE-TX compatible PHY. It provides a glueless 32-bit PCI master interface and supports a 128 Kbyte Flash interface. The package is a thin BGA with a small footprint (15 mm X 15 mm).

The 82559 supports the Intel Preboot Execution Environment (PXE) driver, which allows a new or existing system to boot over the network and download software or an image, including the operating system, stored on a server. The 82559 provides for operating system independent network booting, automating the setting up and configuration of new systems. If the operating system or applications software is damaged, the system can be recovered by downloading the original image from server again, reducing the total cost of maintenance.

5.7.1 Design Note for the Intel® 82559 Fast Ethernet Controller

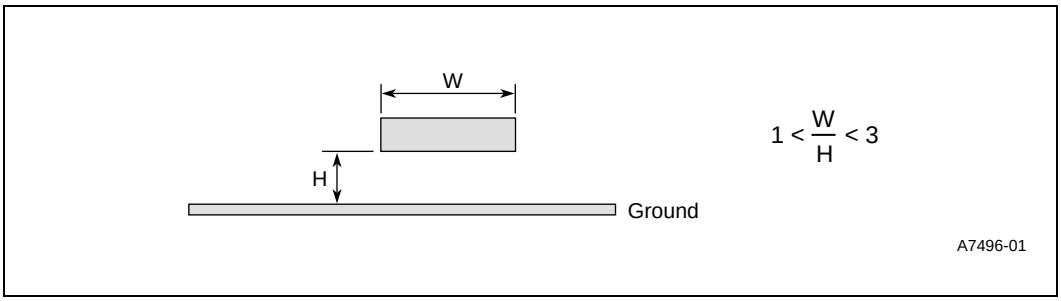
The differential transmit signal pair (TDP/TDN) is terminated with a 100 W (1%) resistor, and the differential receive signal pair (RDP/RDN) is terminated with a 120 W (1%) resistor. These termination resistors should be placed as close to the PHY as possible. These resistors terminate the entire impedance seen at the termination source (for example, the PHY), including the wire impedance reflected through the transformer. Figure 4 depicts the placement of the termination resistors.

Figure 4. Placement of Termination Resistor



The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals, such as the clock, and signal layers that are close to a ground plane or power plane should be as short and as wide as is practical. As shown in Figure 5, this ratio is ideally somewhere between 1:1 and 3:1. To maintain the impedance of a trace, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from a power or ground plane.

Figure 5. Trace Geometry



NOTE: W= Trace Width, H= Height Above Ground Plane

5.7.2 Wired for Management

Wired for Management (WfM) is an Intel initiative to improve the manageability of desktop, mobile, server and embedded systems. The goal of WfM is to reduce the total cost of ownership (TCO) through improved manageability in the following four technology areas:

- Instrumentation
- Remote Service Boot
- Remote Wake-Up
- Power Management

Manageability features in each of these four technology areas combine to form the Wired for Management Baseline Specification. A copy of the Wired for Management Baseline Specification, Version 2.0 can be obtained from:

http://developer.intel.com/ial/wfm/wfmspecs.htm

An on-line Design Guide is available at:

http://developer.intel.com/ial/WfM/design/index.htm

Future versions of the specification will be available at this site.

In the Intel-based electronic classroom reference configuration, the NIC is WfM compliant, particularly in the Remote Service Boot features needed to support the student computing stations' remote boot from the server.

5.7.2.1 Instrumentation

A component's instrumentation consists of code that maintains attributes with up-to-the-minute values and adjusts the component's operational characteristics based on these values. By providing instrumentation, the platform provides accurate data to management applications, so those applications can make the best decisions for managing a system or product. The WfM 2.0 Baseline requires that compliant desktop and mobile platforms utilize the DMI Version 2.00 Management Interface (MI) and Component Interface (CI) application programming interfaces and host a DMI v2.00 Service Provider, as defined by the DMTF. Intel's DMI 2.0 Service Provider Software Development Kit (SDK) provides a DMI Service Provider and binaries that support DMI Version 2.00. This kit is available at the following URL:

http://developer.intel.com/ial/WfM/tools/sdk/index.htm

Intel® LANDesk® Client Manager product includes the Service Provider and component instrumentation. Information regarding this product can be found at:

http://developer.intel.com/ial/WfM/tools/ldcm/index.htm

The WfM Baseline Instrumentation specification identifies specific DMI standard groups, including event generation groups, that must be instrumented for a Baseline-compliant platform. This specification provides support for the SMBIOS revision 2.0 specification that along with appropriate component instrumentation will supply some of the required data in the specified DMI 2.0 groups.

5.7.2.2 Remote Service Boot

The WfM Baseline specifies the protocols by which a client requests and downloads an executable image from a server and the minimum requirements on the client execution environment when the downloaded image is executed. The Baseline specification includes a set of APIs for the particular network controller used. The code supporting the Preboot eXecution Environment (PXE) and the network controller is provided on the EtherExpress™ PRO/100 WfM adapters Option ROM. Two implementation options are available:

- NIC with Option ROM and Wake on LAN Header
- LAN on Motherboard implementation.

  For this option, the Preboot execution environment and the network controller code must be incorporated into the system BIOS.

In addition, the BIOS must provide the _SYSID_ and _UUID_ data structures. The details of the BIOS requirements can be obtained from the Intel web site:

http://developer.intel.com/ial/WfM/design/pxedt/index.htm

5.7.2.3 Remote Wake-Up

If a student computing station supports a reduced power state, it is possible to bring the system to a fully powered state in which all power management interfaces are available. Typically, the LAN adapter recognizes a special packet as a signal to wake up the system. The system BIOS must enable the wake event and provide wake up status. The details of the BIOS requirements can be obtained from the Intel web site:

http://developer.intel.com/ial/WfM/design/rwudt/index.htm

5.7.2.4 Power Management

WfM Baseline compliant systems have four distinct power states: Working, Sleeping, Soft Off, and Mechanical Off. A user accessible switch that will send a soft off request to the system usually provides Soft Off. A second optional “override” switch located in a less obvious place (or removal of the power cord) stops current flow forcing the platform into the mechanical off state without OS consent. Note that a second “override” switch is required for legal reasons in some jurisdictions (for example, some European countries). The BIOS may support the power management requirement either through the APM revision 1.2 or ACPI revision 1.0 specifications. See Intel's web site for additional information:

http://developer.intel.com/ial/WfM/design/pmdt/index.htm.

5.8 Low Pin Count (LPC) Interface

In the Intel 810 chipset platform, the Super I/O* (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, a floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC’97 interface does not provide support for a game port. In systems that have ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of devices offered and features supported.

6.0 Conclusion

Traditional teaching media such as projector, video player, audio recorder, and black board are being replaced in the Intel-based electronic classroom by new computer-based teaching media. Audio, video and 2-D/3-D graphics can be introduced in the Intel-based electronic classroom. The classroom can be connected to the Internet by using modem or Intel router.

Intel provides the building blocks for Intel-based electronic classroom systems that feature manageability, ease of maintenance, compatibility with operating systems and application software, and long life cycle support for the Intel components. The recommended motherboard configuration is designed to optimize the performance of the overall system, reducing board space, power consumption, and the total cost of ownership.

Appendix A References

Document	Order Number / URL
Intel Documents and Resources	
Intel® 810 Chipset Design Guide	Order Number 290657 http://developer.intel.com/design/chipsets/designex/290657.htm
Intel® 82810 Chipset: Intel 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) datasheet	Order Number 290656 http://developer.intel.com/design/chipsets/datashts/290656.htm
Intel® 82801AA (ICH) and Intel 82801AB (ICH0) I/O Controller Hub datasheet	Order Number 290655 http://developer.intel.com/design/chipsets/datashts/290655.htm
Intel® 82801 FirmWare Hub (FWH) datasheet	Order Number 290658 http://developer.intel.com/design/chipsets/datashts/290658.htm
Intel® Celeron™ Processor datasheet	Order Number 243658 http://developer.intel.com/design/celeron/datashts/243658.htm
VRM 8.2 DC-DC Converter Design Guidelines	Order Number 243733 http://developer.intel.com/design/pentiumii/xeon/designgd/243773.htm
AP-585 Pentium® II Processor GTL+ Guidelines	Order Number 243330 http://developer.intel.com/design/pentiumii/applnots/243330.htm
AP-587: Slot 1 Processor Power Distribution Guidelines	Order Number http://developer.intel.com/design/celeron/applnots/243332.htm
Pentium® II Processor Developer's Manual	Order Number 243341 http://developer.intel.com/design/PentiumII/manuals/243502.htm
Pentium® II Processor at 350 MHz, 400 MHz and 450 MHz datasheet	Order Number 243657 http://developer.intel.com/design/PentiumII/datashts/243657.htm
Intel® 82559 Fast Ethernet Multifunction PCI Controller	http://developer.intel.com/design/network/82559.htm
AP-399 82559 Printed Circuit Board Design	Order Number 739073 http://developer.intel.com/design/network/applnots/739073.htm
AP-392 82559 LAN on Motherboard (LOM) Design Guide	Order Number 718213 http://developer.intel.com/design/network/applnots/718213.htm
Intel® Networking LANSchool software site	http://www.intel.com/network/products/lanschool.htm
AC'97 Specifications on Intel web site	http://developer.intel.com/pc-supp/platform/ac97/index.htm
Wired for Management specifications and information	http://developer.intel.com/ial/wfm/index.htm
Non-Intel Documents and Resources	
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/
Universal Serial Bus Specification, Revision 1.0	http://www.usb.org/

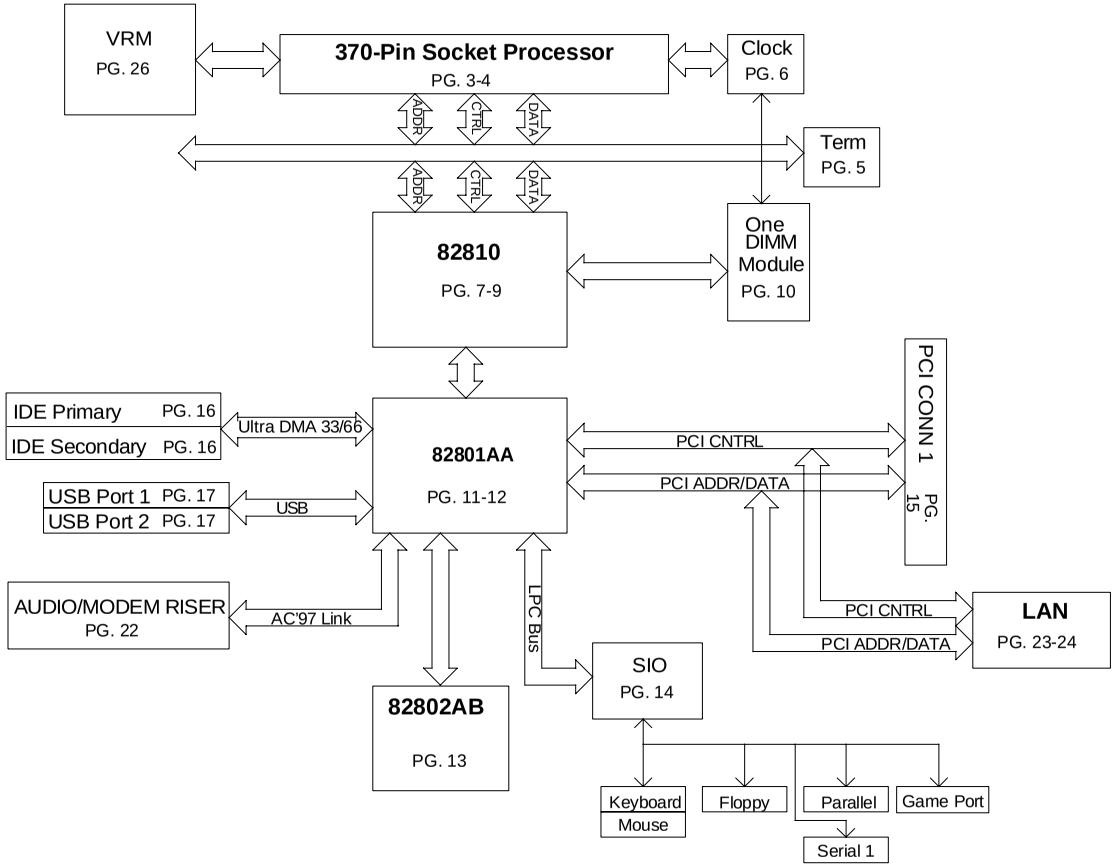
Appendix B Intel-Based Electronic Classroom Schematics

Intel® Celeron™ Processor And Intel® 810 Based Electronic Classroom Student Computing Station Hardware Schematics

** Please note these schematics are subject to change.

Electronic Classroom Student Computing Station Ref Schematic COVER SHEET	Rev 0.1
INTEL CORPORATION APPLIED COMPUTING PRODUCTS DIVISION 5000 W CHANDLER BLVD. CH6-236 CHANDLER, AZ 85226	Last Revision Date: Sheet: 1 of 33

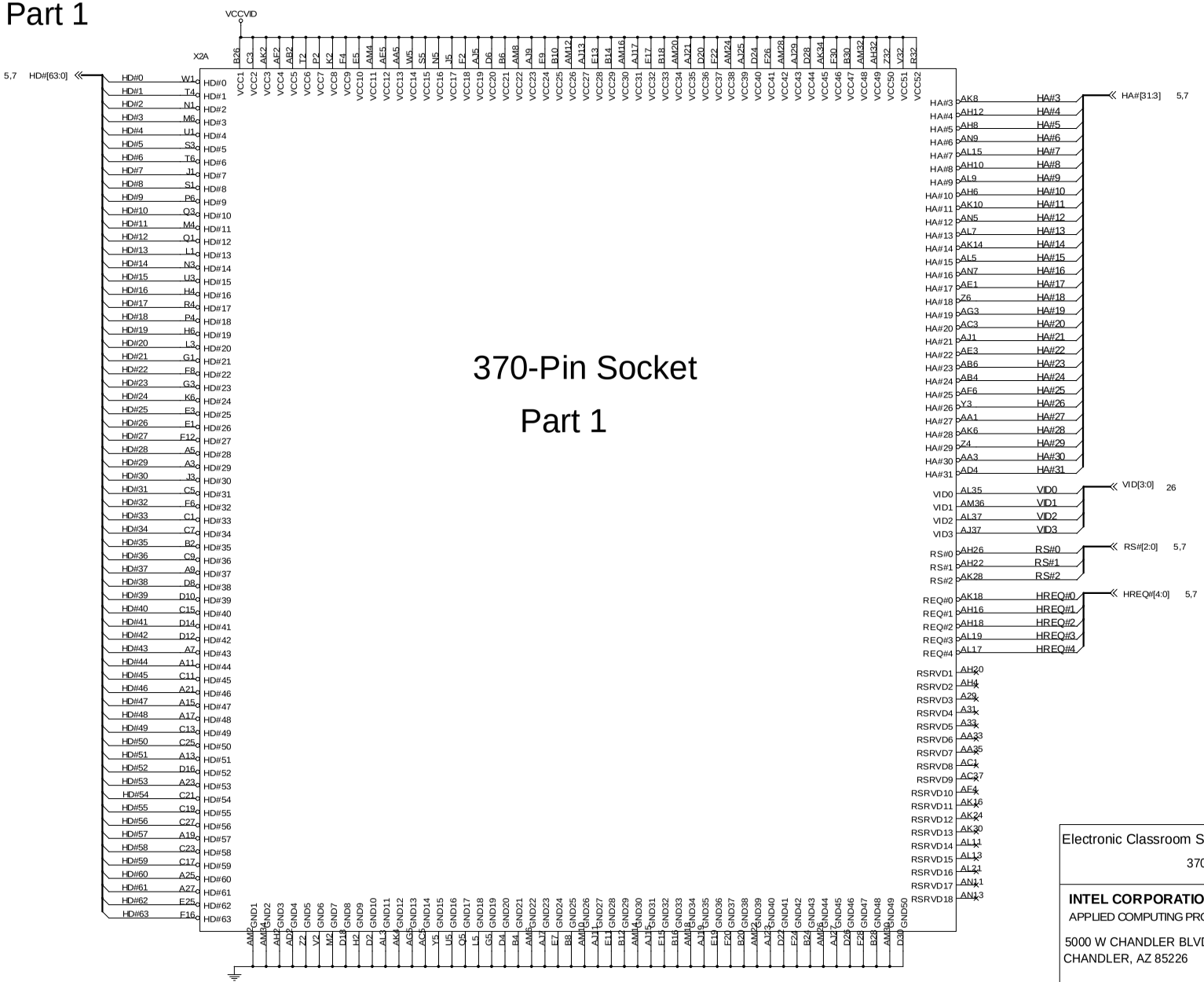
Block Diagram



Electronic Clasroom Student Computing Station Ref. Schematic BLOCK DIAGRAM	REV 0.1
INTEL CORPORATION APPLIED COMPUTING PRODUCTS DIVISION 5000 W CHANDLER BLVD. CH6-236 CHANDLER, AZ 85226	Last Revision Date: Sheet: 2 of 33

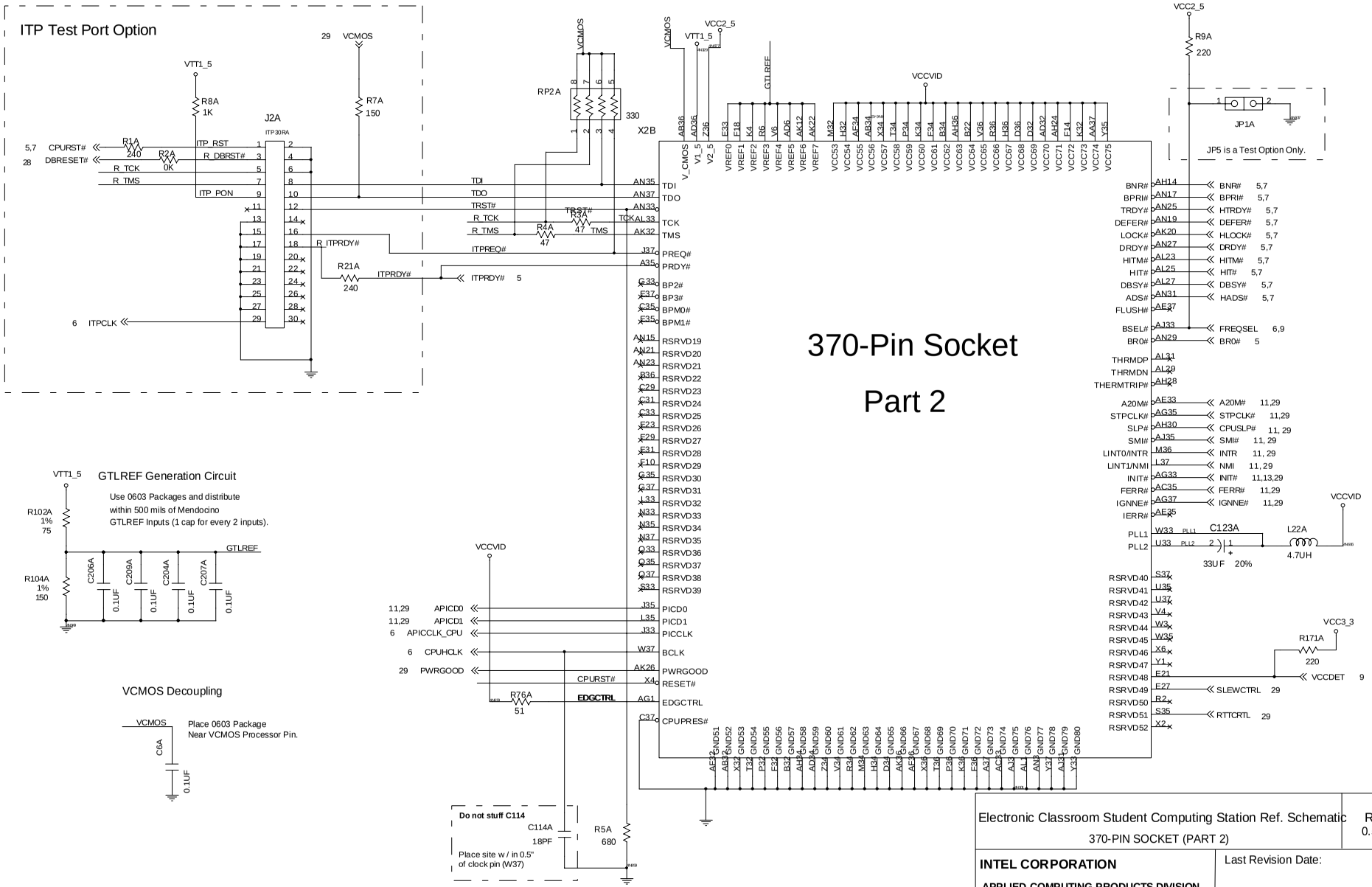
370PGA Socket

Part 1



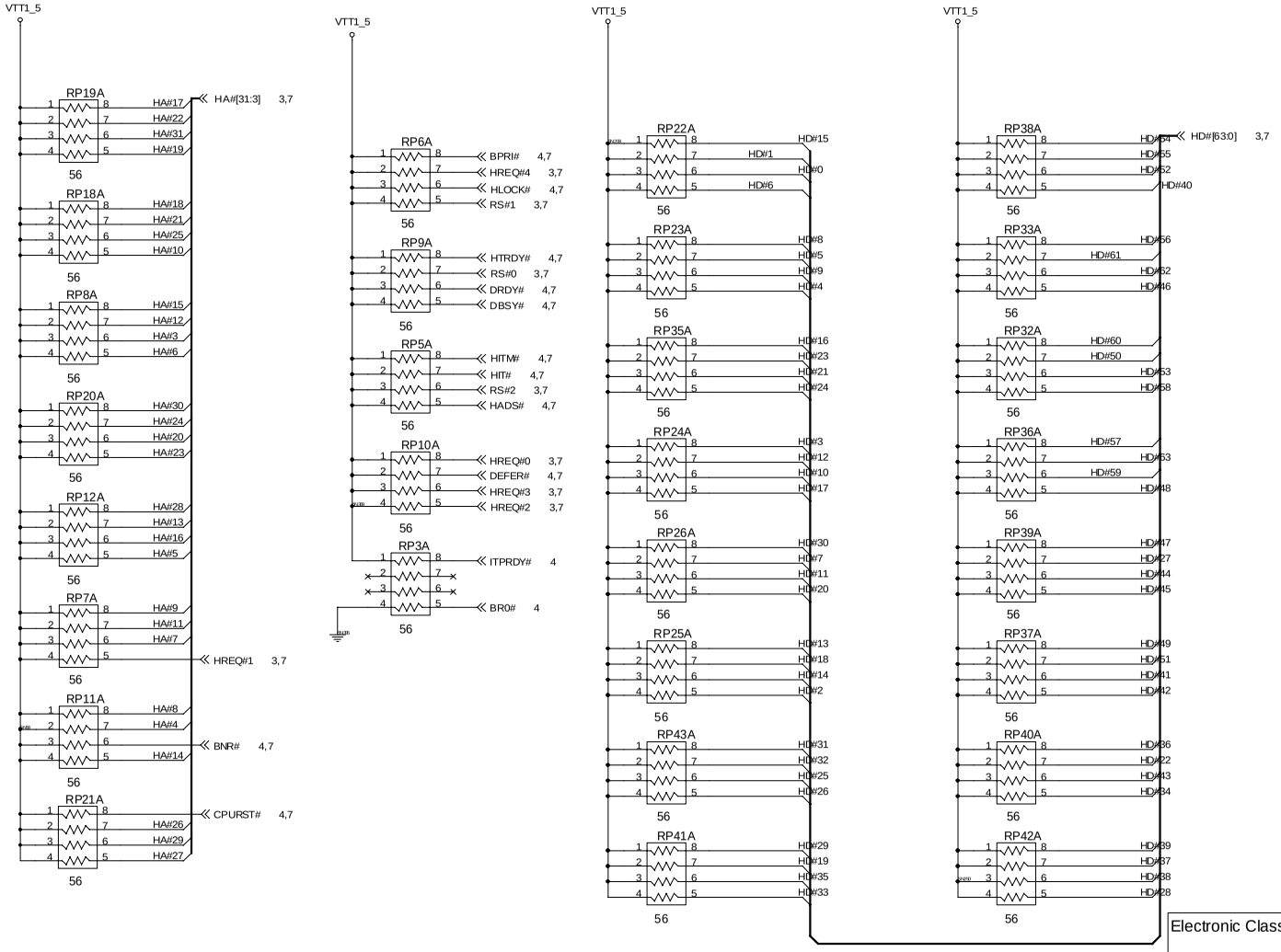
Electronic Classroom Student Computing Station Ref. Schematic 370-PIN SOCKET (PART 1)	REV. 0.1
INTEL CORPORATION APPLIED COMPUTING PRODUCTS DIVISION 5000 W CHANDLER BLVD. CH6-236 CHANDLER, AZ 85226	Last Revision Date: Sheet: 3 of 33

370PGA Socket
Part 2



Electronic Classroom Student Computing Station Ref. Schematic 370-PIN SOCKET (PART 2)	Rev 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 4 of 33

GTL Termination



Electronic Classroom Student Computing Station Ref. Schematic GTL TERMINATION		REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
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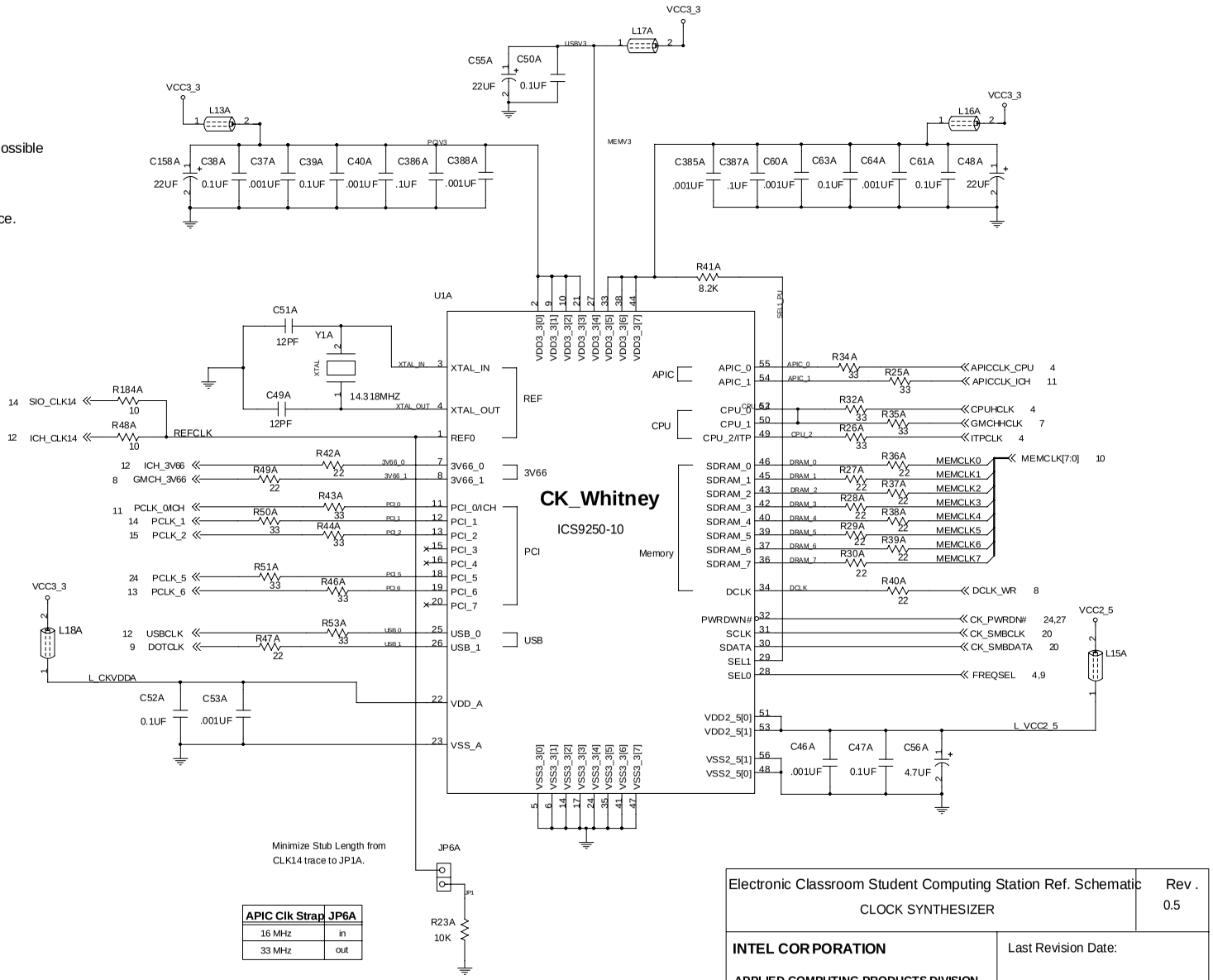
Clock Synthesizer

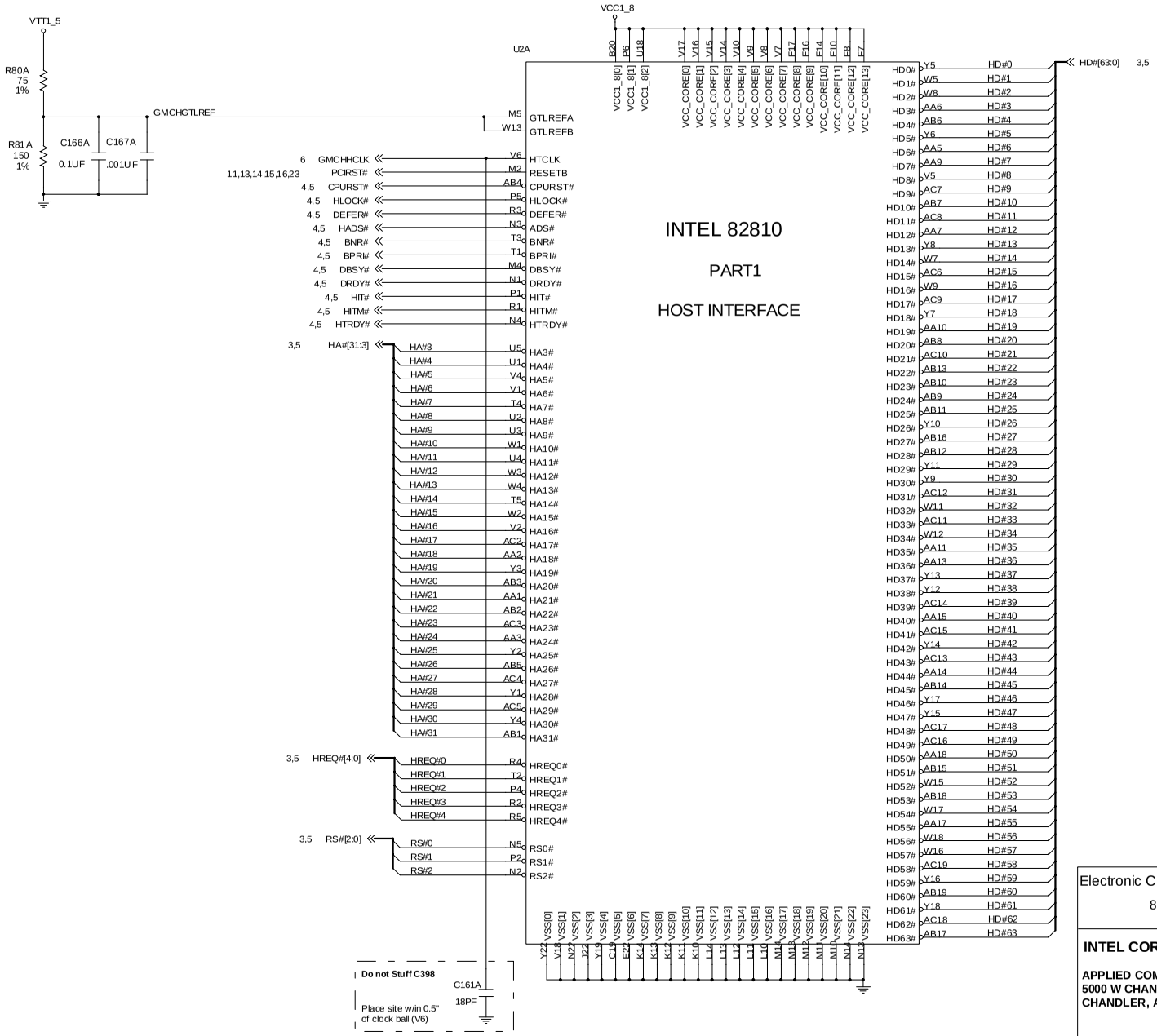
Notes:

- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin has to go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.



Electronic Classroom Student Computing Station Ref. Schematic CLOCK SYNTHESIZER	Rev . 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 6 of 33

82810, PART 1: HOST INTERFACE



Electronic Classroom Student Computing Station Ref. Schematic 82810 ,PART 1: HOST INTERFACE		Rev . 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
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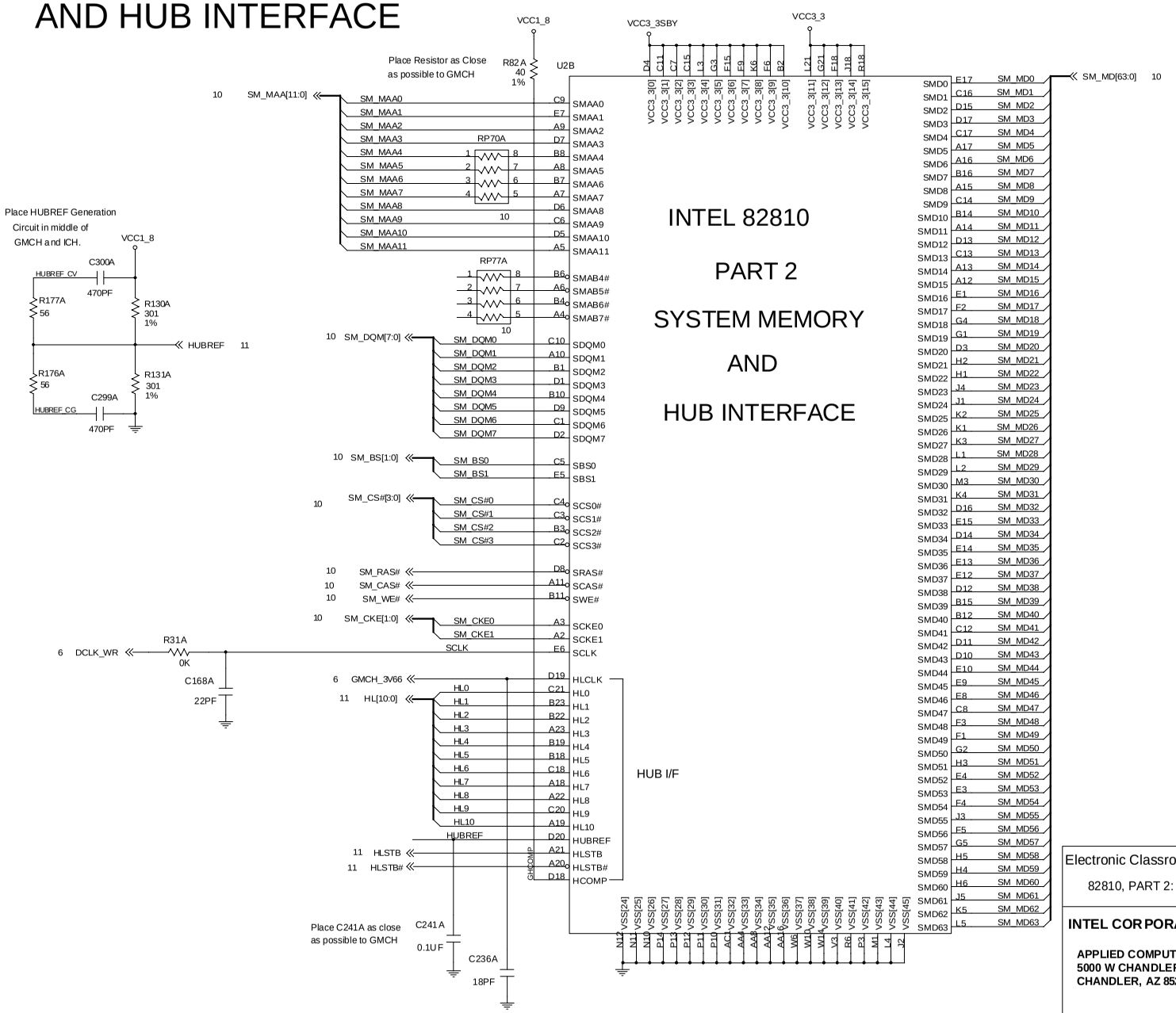
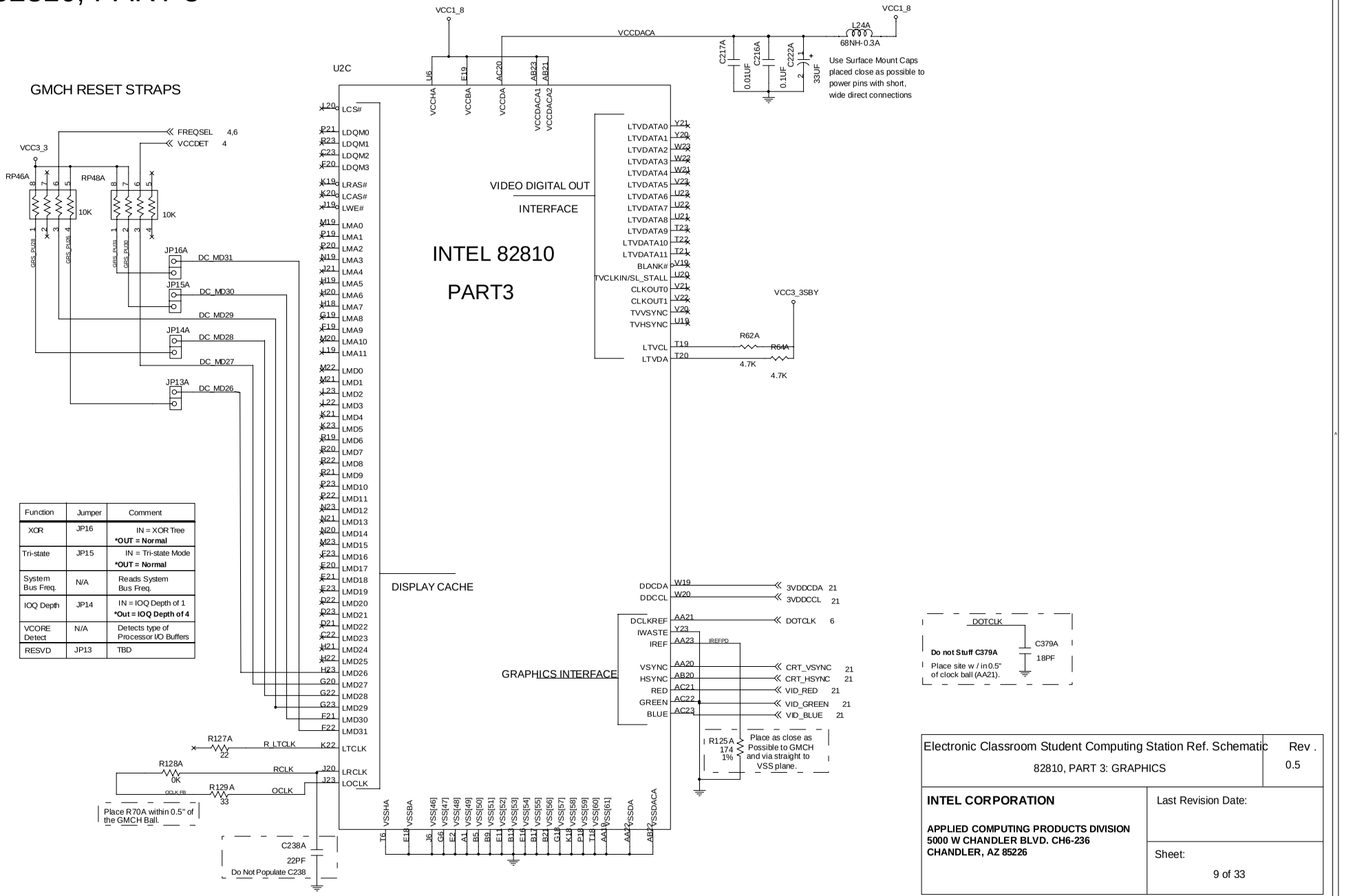
82810, PART 2: SYSTEM MEMORY AND HUB INTERFACE



Electronic Classroom Student Computing Station Ref. Schematic 82810, PART 2: SYSTEM MEMORY AND HUB INTERFACE	Rev . 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 8 of 33

JP16

82810, PART 3



Function	Jumper	Comment
XOR	JP16	IN = XOR Tree ***OUT = Normal**
Tri-state	JP15	IN = Tri-state Mode ***OUT = Normal**
System Bus Freq.	N/A	Reads System Bus Freq.
IOQ Depth	JP14	IN = IOQ Depth of 1 ***Out = IOQ Depth of 4**
VCORE Detect	N/A	Detects type of Processor I/O Buffers
RESVD	JP13	TBD

Electronic Classroom Student Computing Station Ref. Schematic 82810, PART 3: GRAPHICS		Rev . 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
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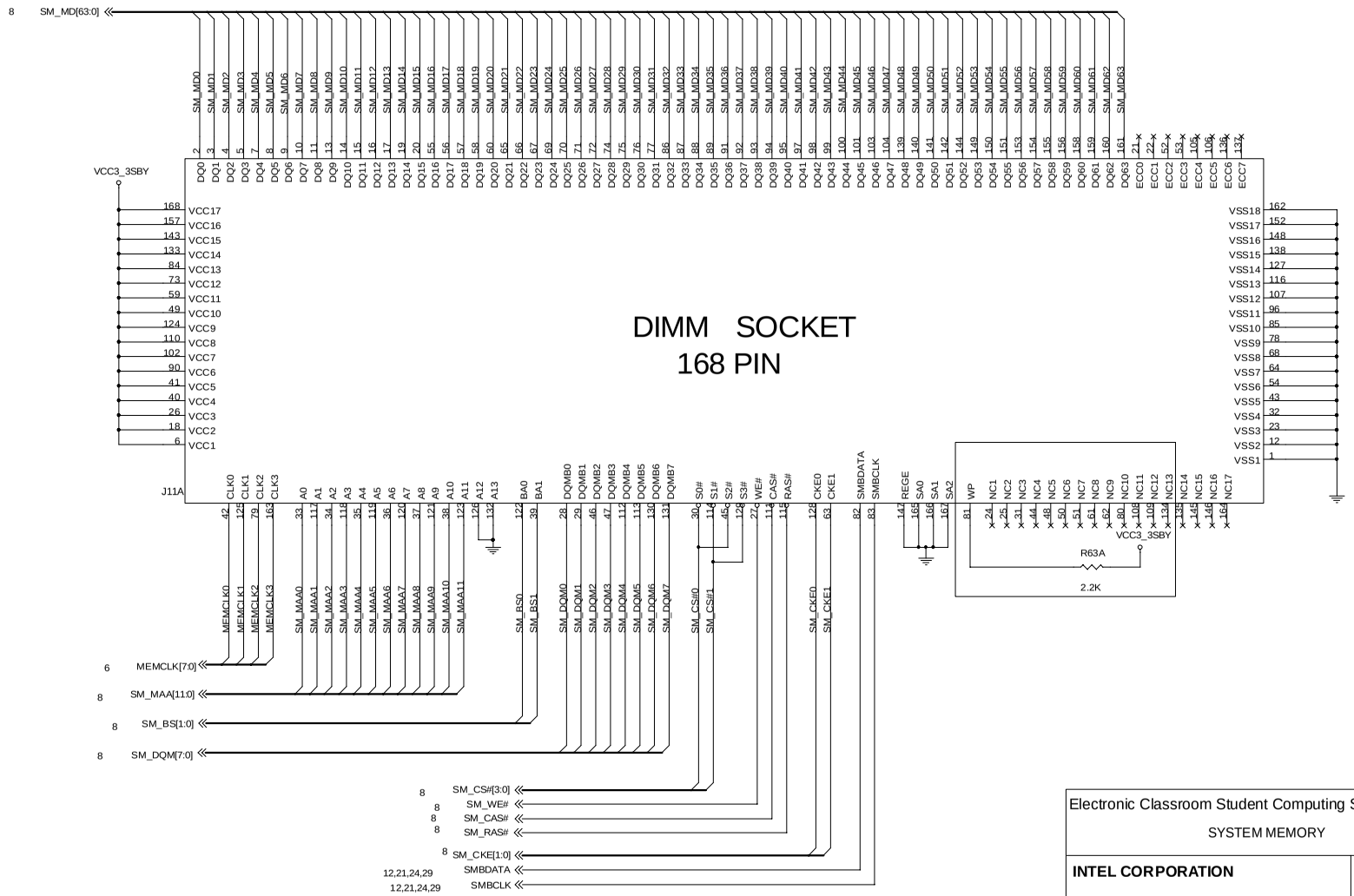
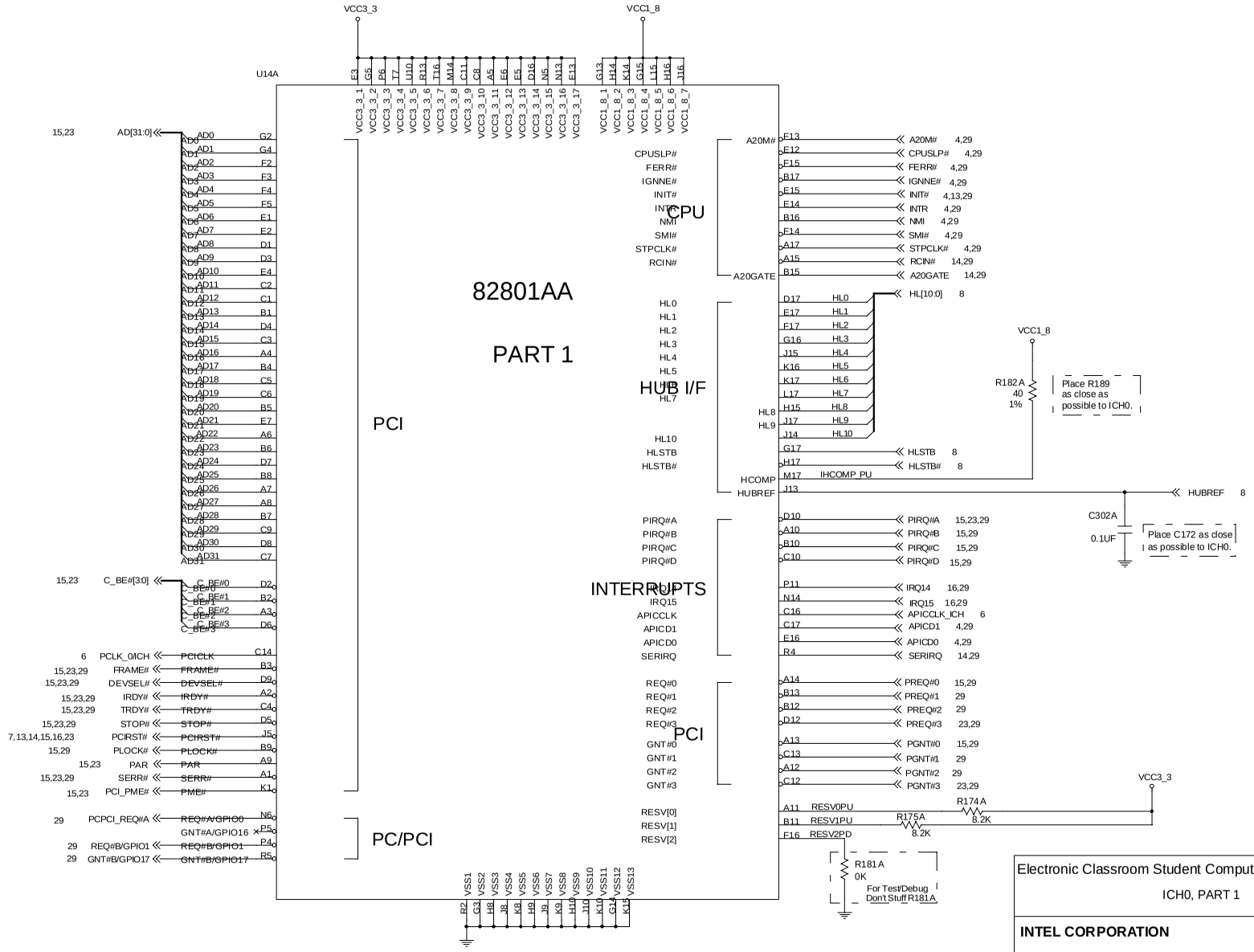
SYSTEM MEMORY



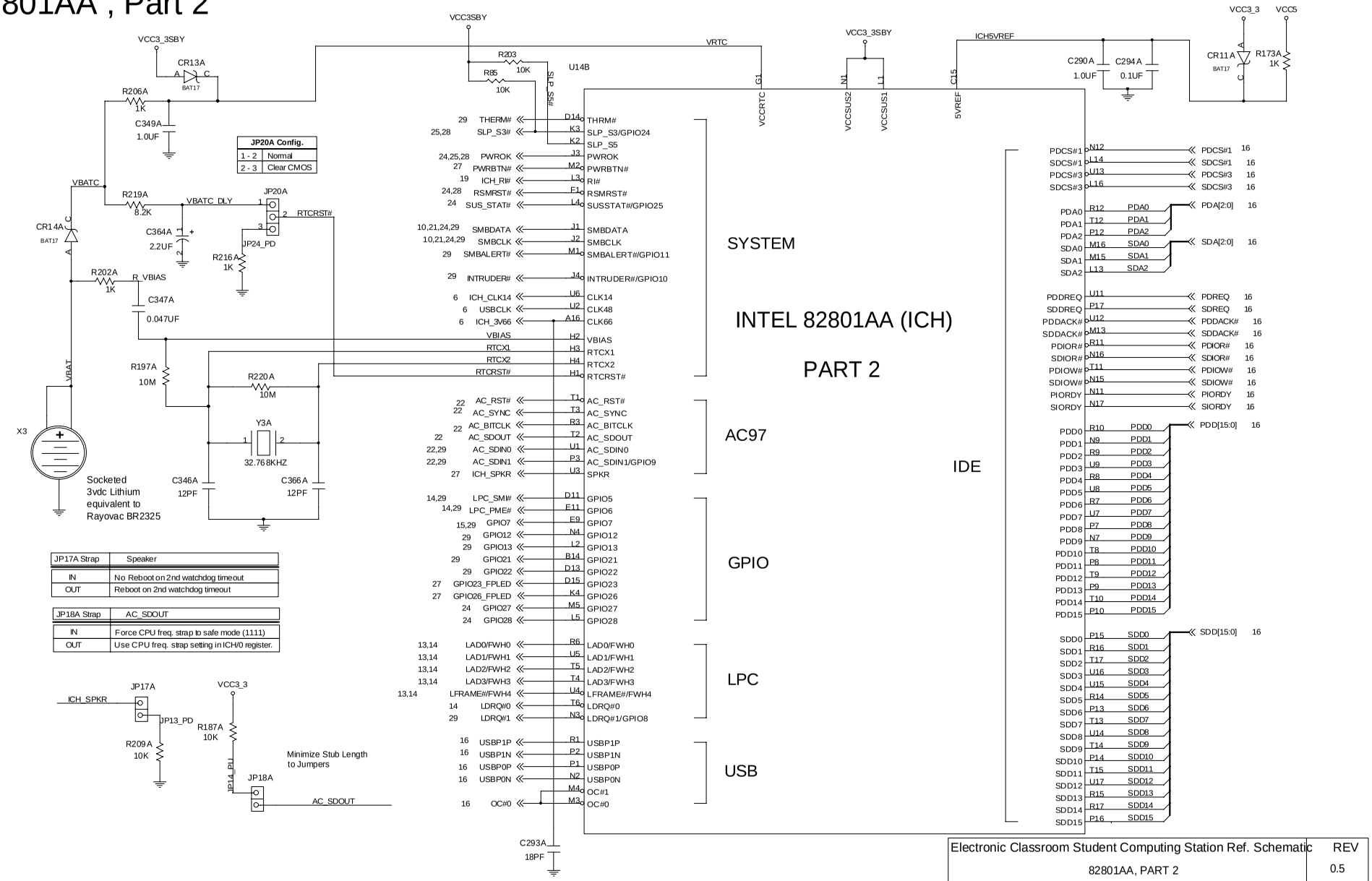
Electronic Classroom Student Computing Station Ref. Schematic SYSTEM MEMORY	REV 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 10 of 33

82801AA , Part 1



Electronic Classroom Student Computing Station Ref. Schematic ICH0, PART 1	REV 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 11 of 33

82801AA , Part 2

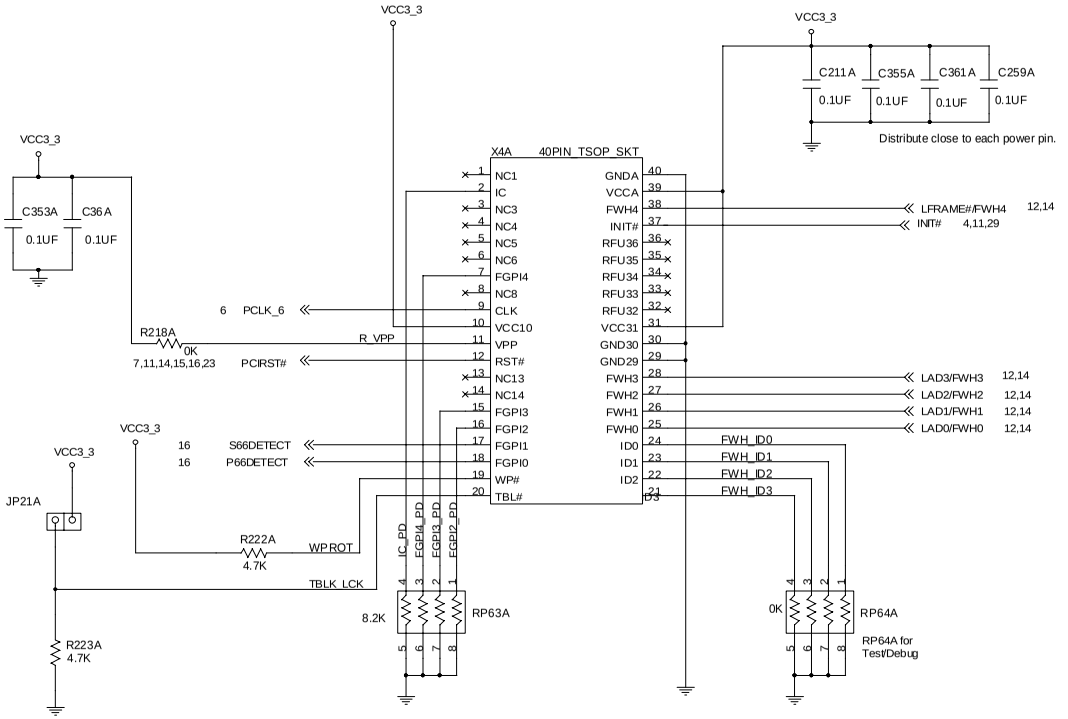


Electronic Classroom Student Computing Station Ref. Schematic	REV
82801AA, PART 2	0.5

INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 12 of 33

FirmWare Hub (82802AB) Socket

NOTE: This is a Socketed Implementation



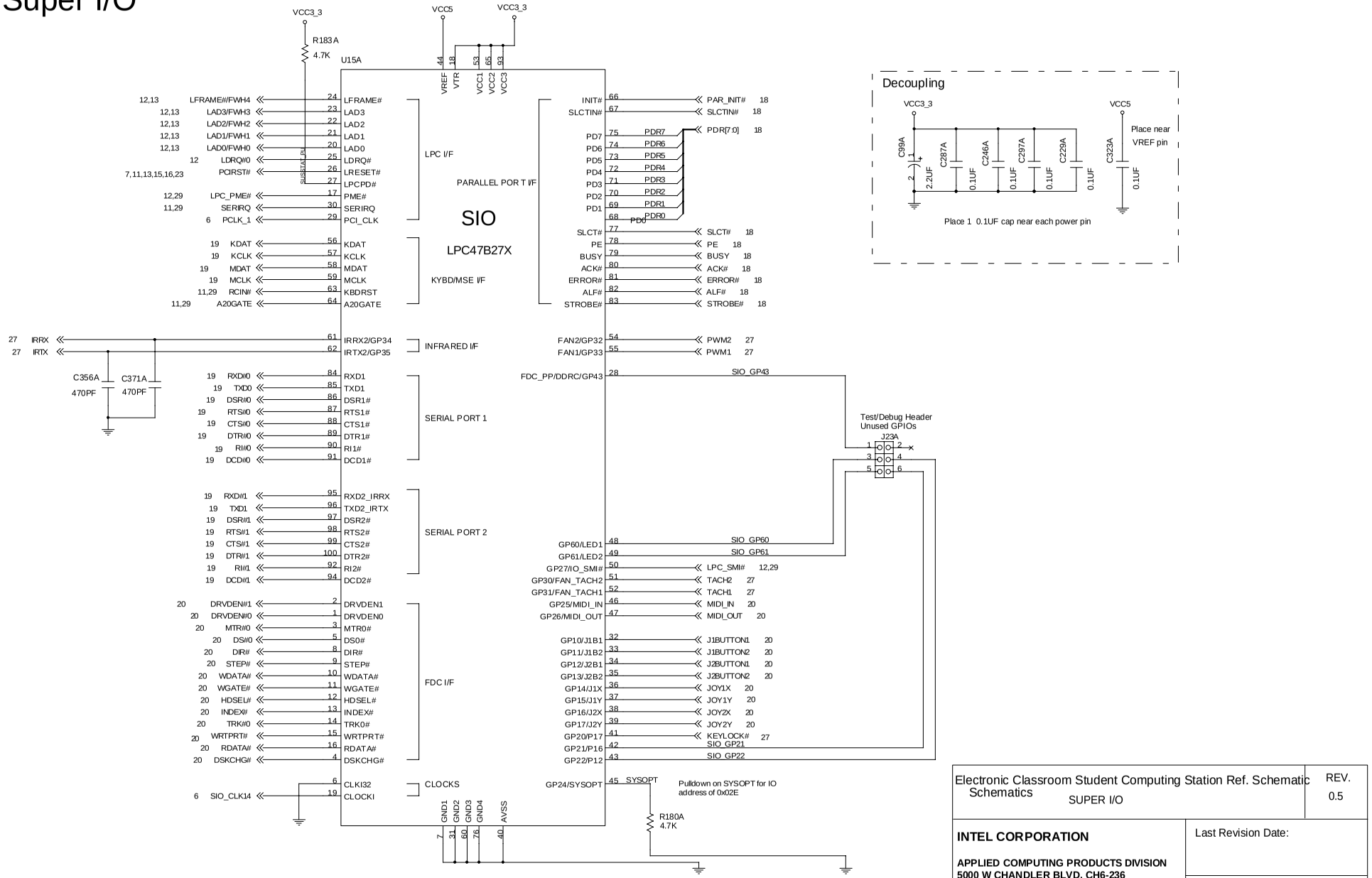
JP21A CONFIG		
IN	Unlocked	
OUT	Locked	Default

Notes:

VPP and WP# are tied to 3.3v
in this configruation Write Protection is register based
with the exception of the Boot Block.

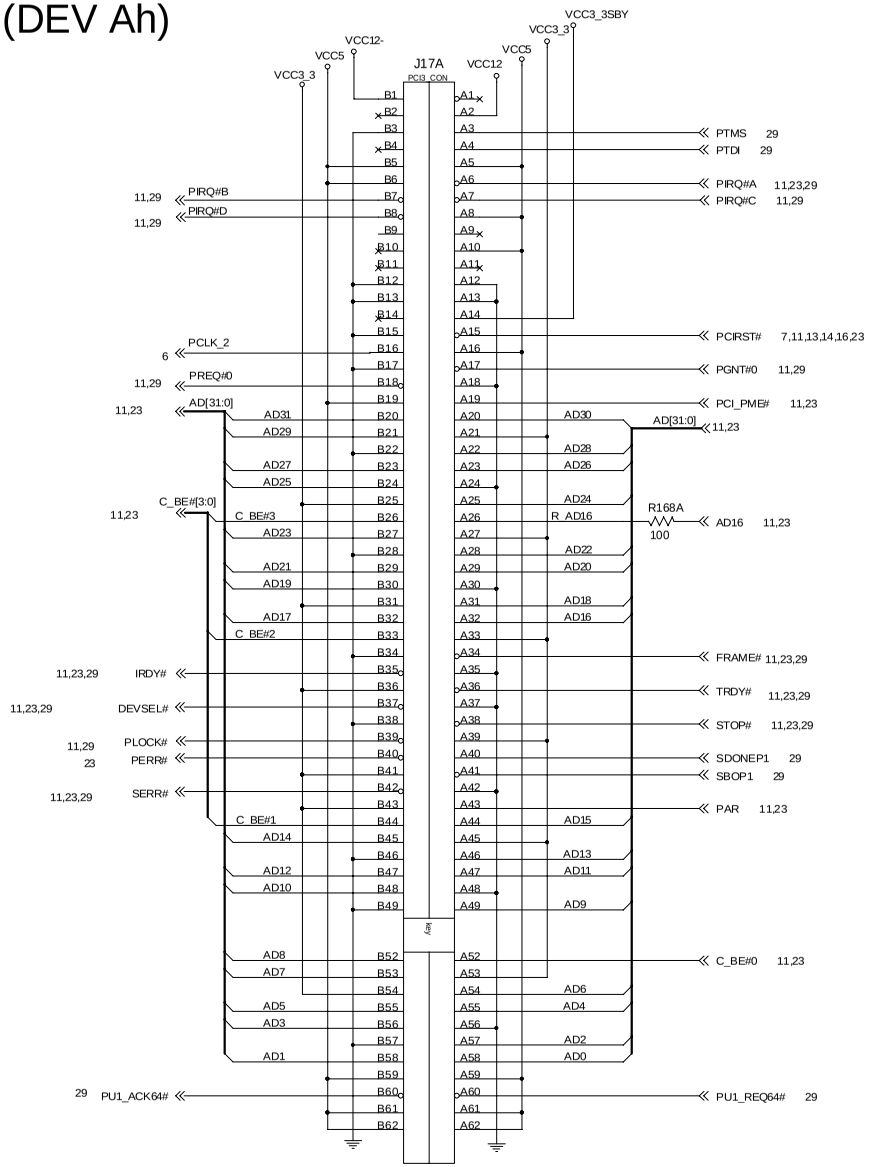
Electronic Classroom Student Computing Station Ref. Schematic FIRMWARE HUB (FWH)	REV 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 13 of 33

Super I/O



Electronic Classroom Student Computing Station Ref. Schematic Schematics SUPER I/O	REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 14 of 33

PCI Connector 0
(DEV Ah)



Electronic Classroom Student Computing Station Ref. Schematic PCI Connector		REV 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
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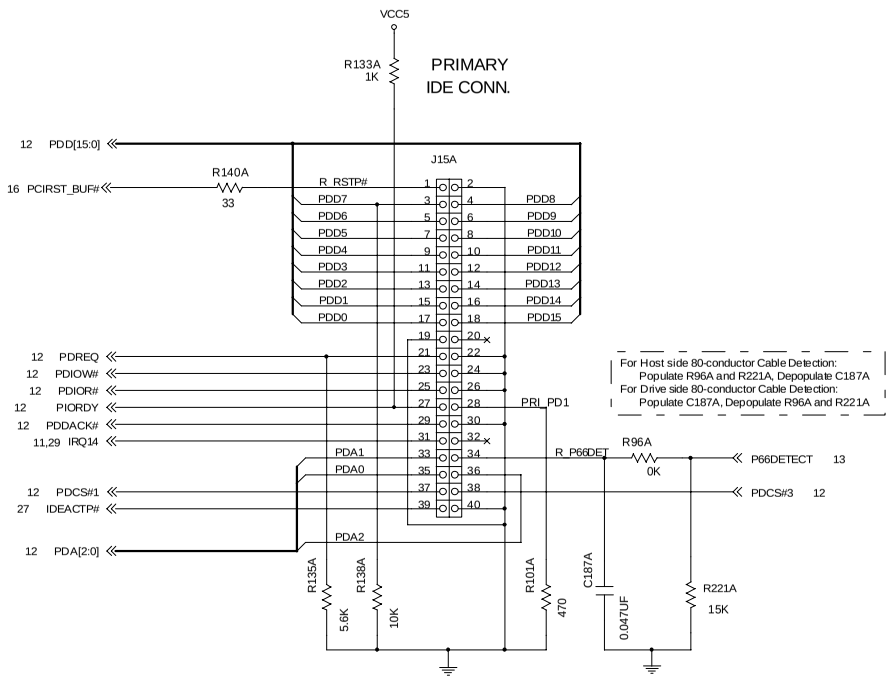
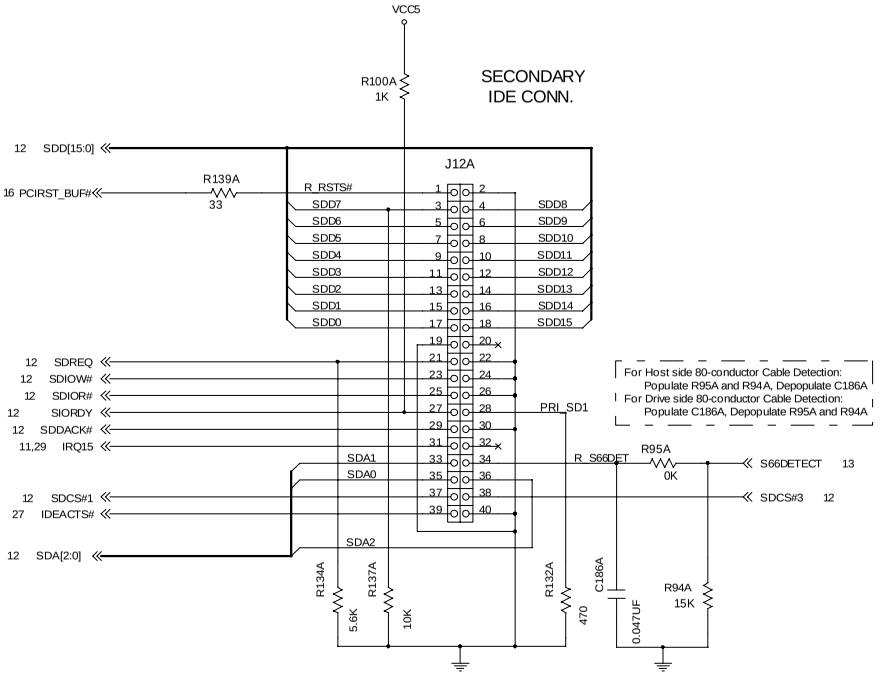
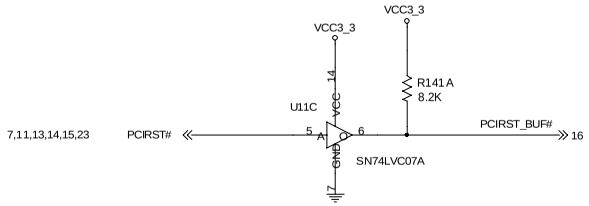
ATA33/66 IDE CONNECTORS

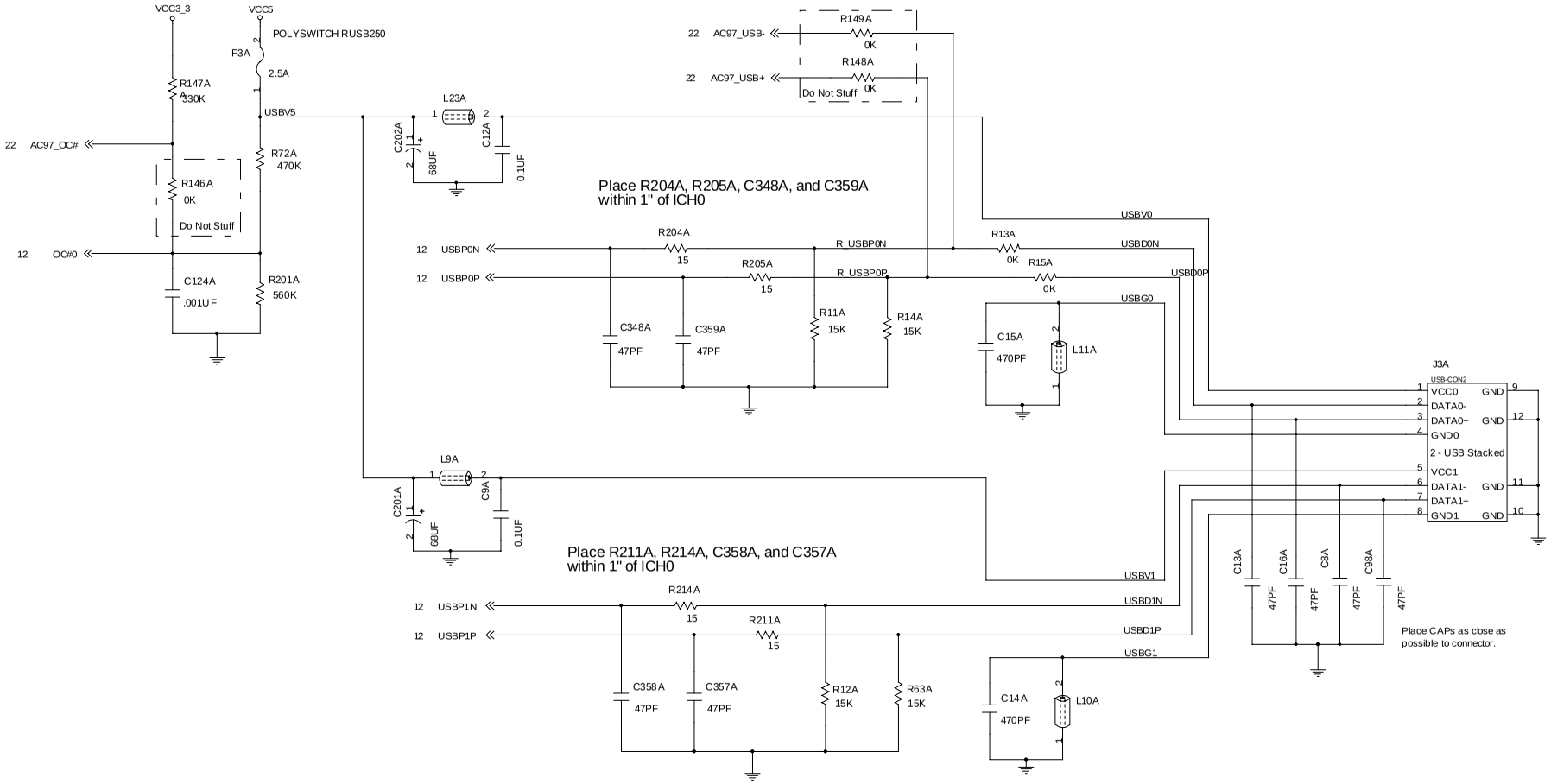






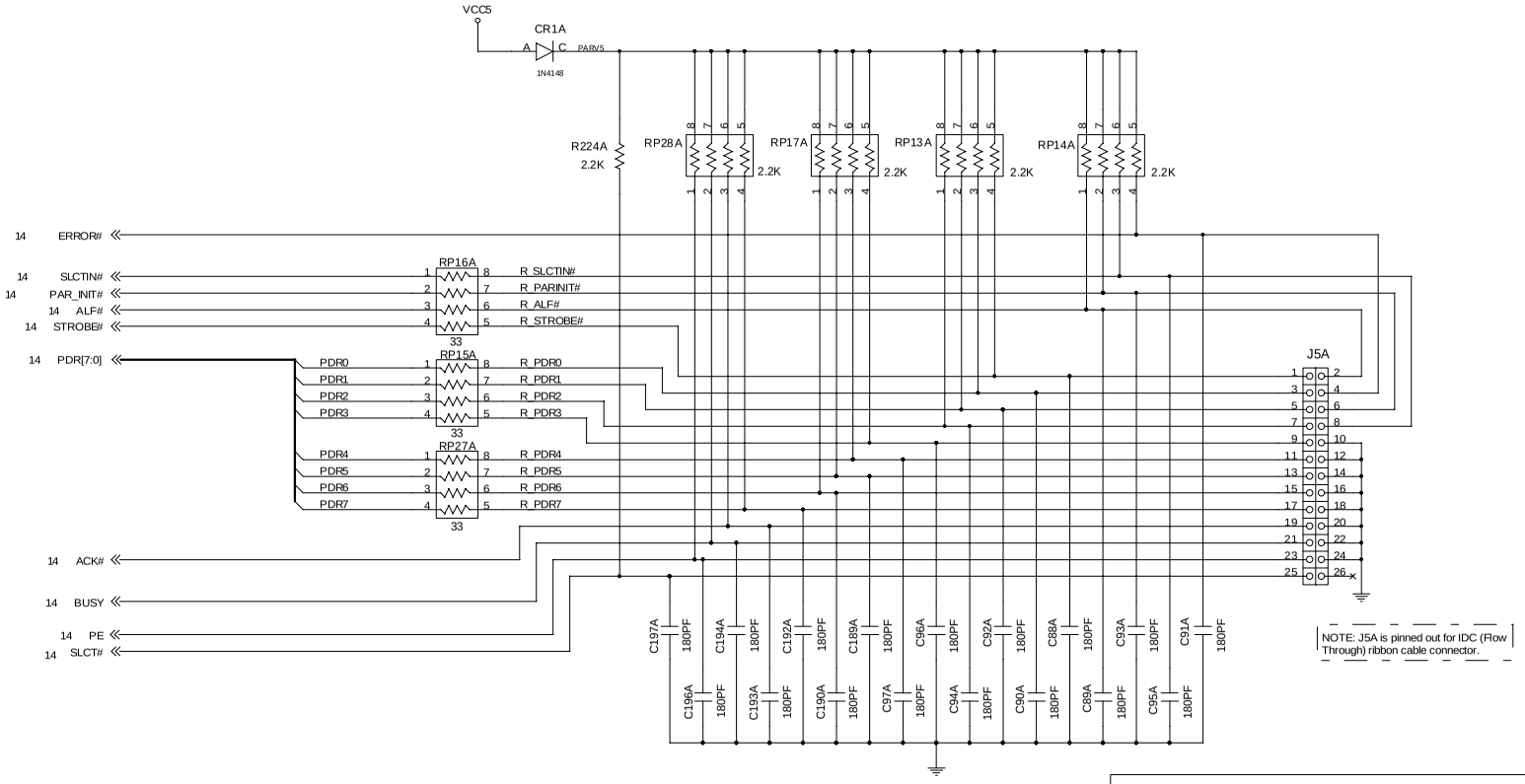
Electronic Classroom Student Computing Station Ref. Schematic ULTRA ATA/33 IDE CONNECTORS		REV. 0.1
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
	Sheet: 16 of 33	

USB Connectors



Electronic Classroom Student Computing Station Ref. Schematic USB CONNECTORS	REV. 0.1
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 17 of 33

Parallel Port Header



Electronic Classroom Student Computing Station Ref. Schematic PARALLEL PORT HEADER		REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date:	
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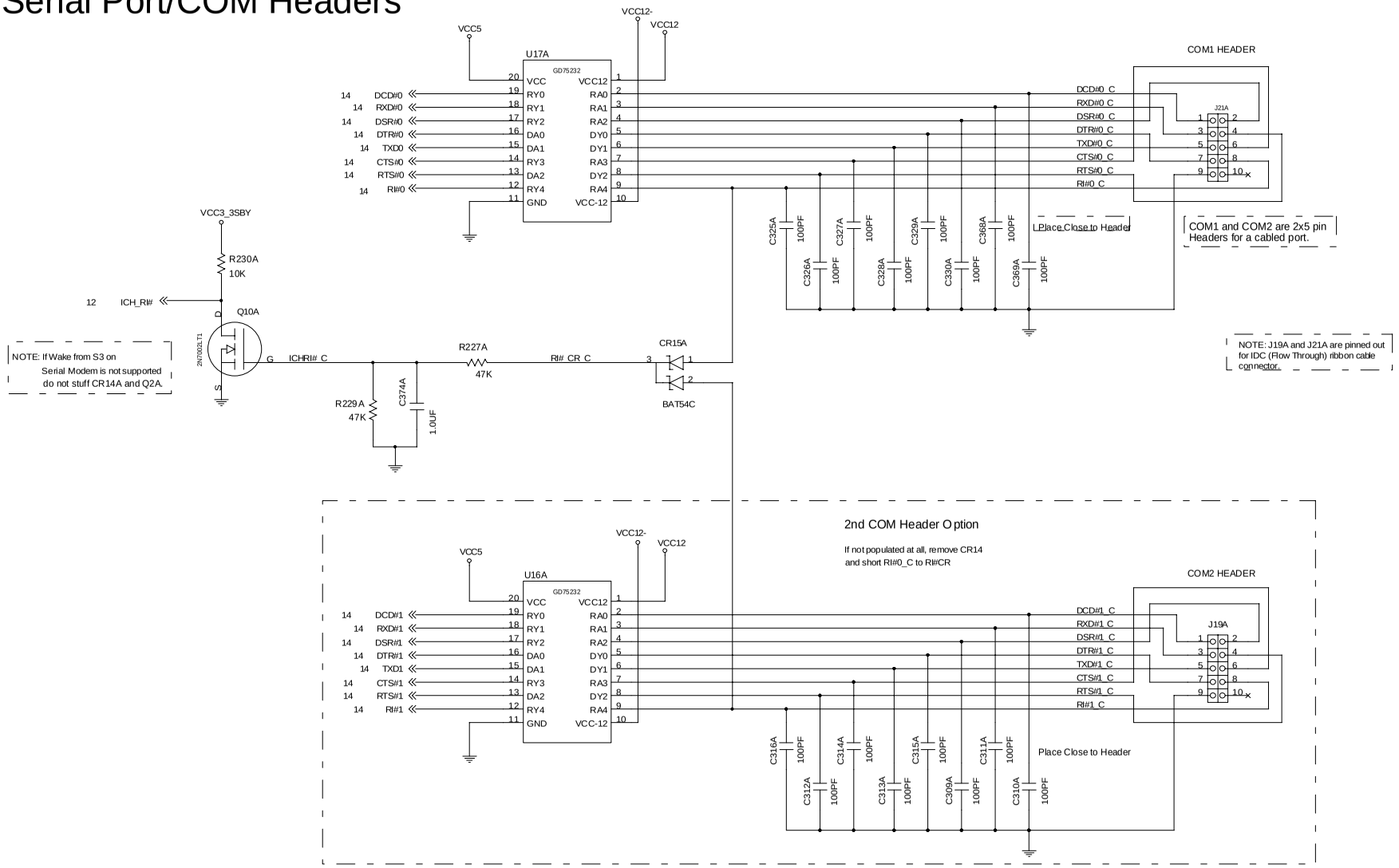
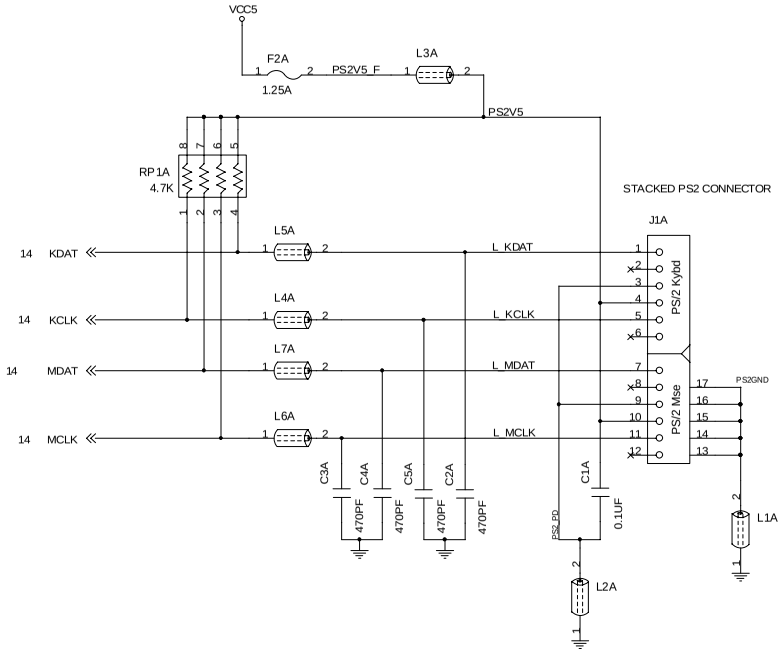
Serial Port/COM Headers

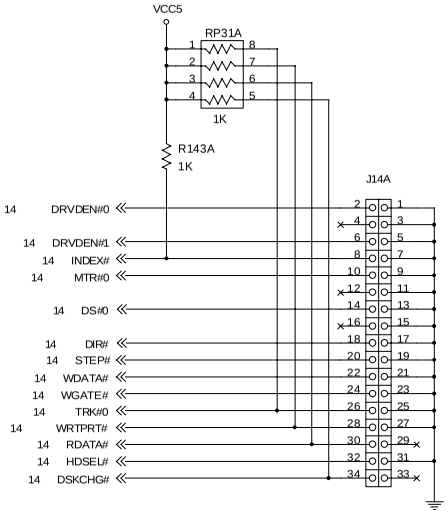


Electronic Classroom Student Computing Station Ref. Schematic SERIAL PORT/ COM HEADERS	REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 19 of 33

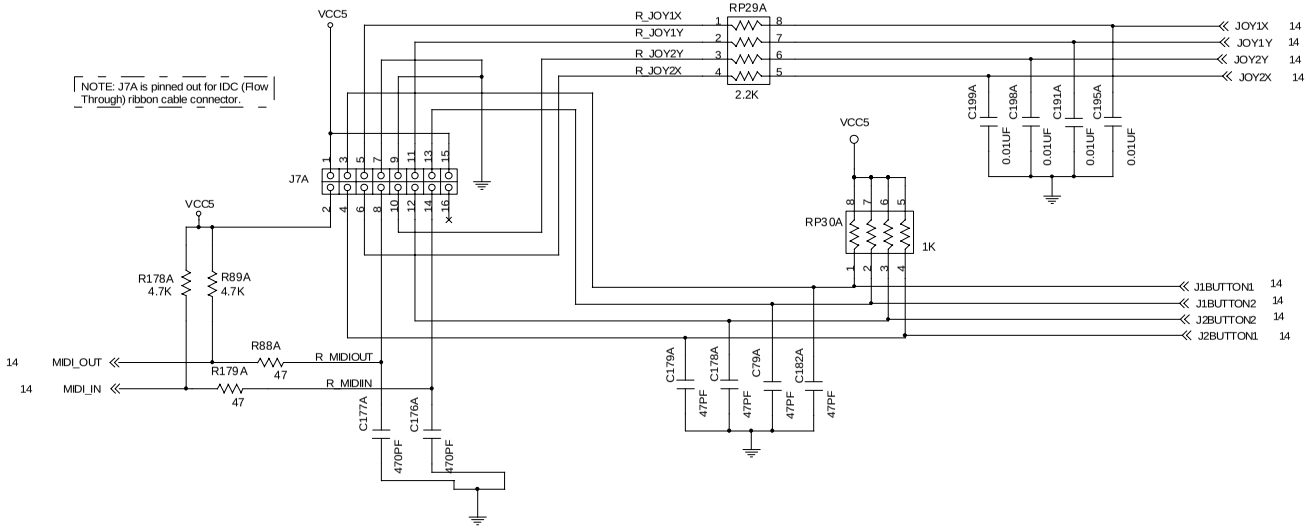
KEYBOARD/MOUSE PORTS



FLOPPY DISK HEADER



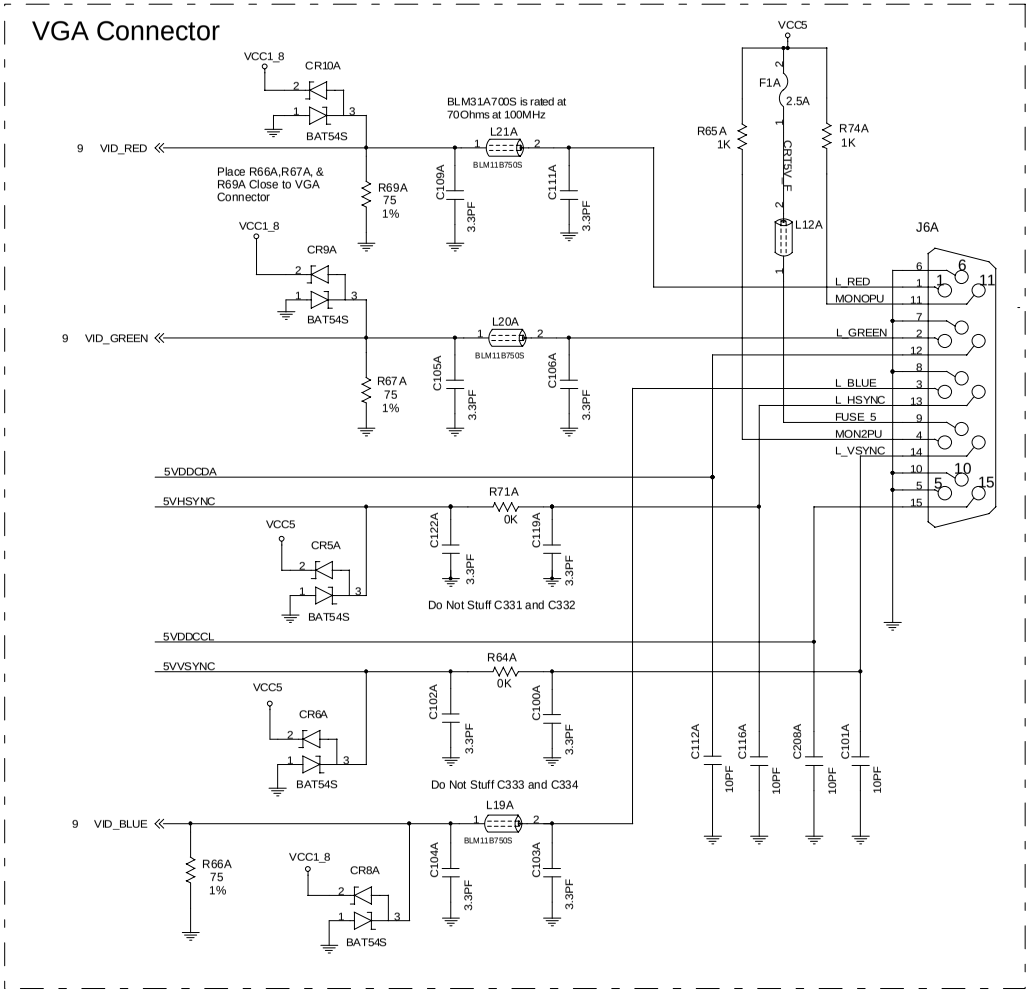
GAME PORT HEADER



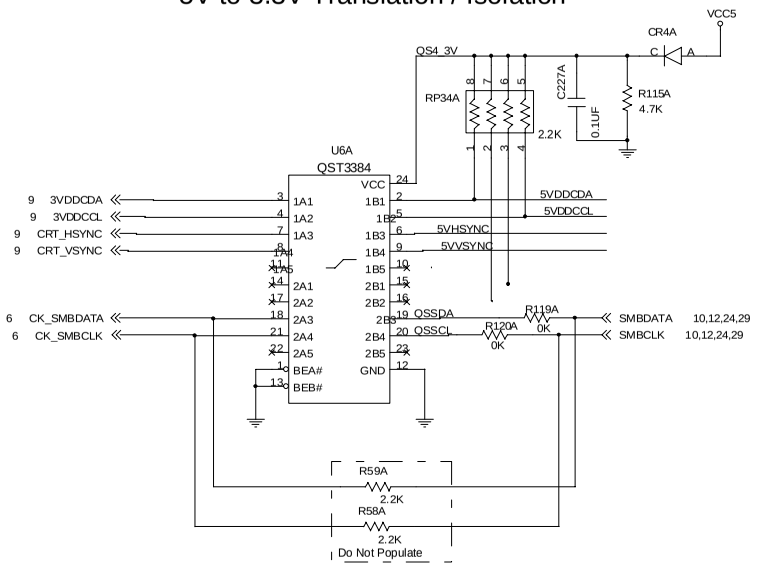
Electronic Classroom Student Computing Station Ref. Schematic KEYBOARD/MOUSE PORTS, FLOPPY DISK HEADER, GAME PORT HEADER	REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 20 of 33

Video Connectors

VGA Connector

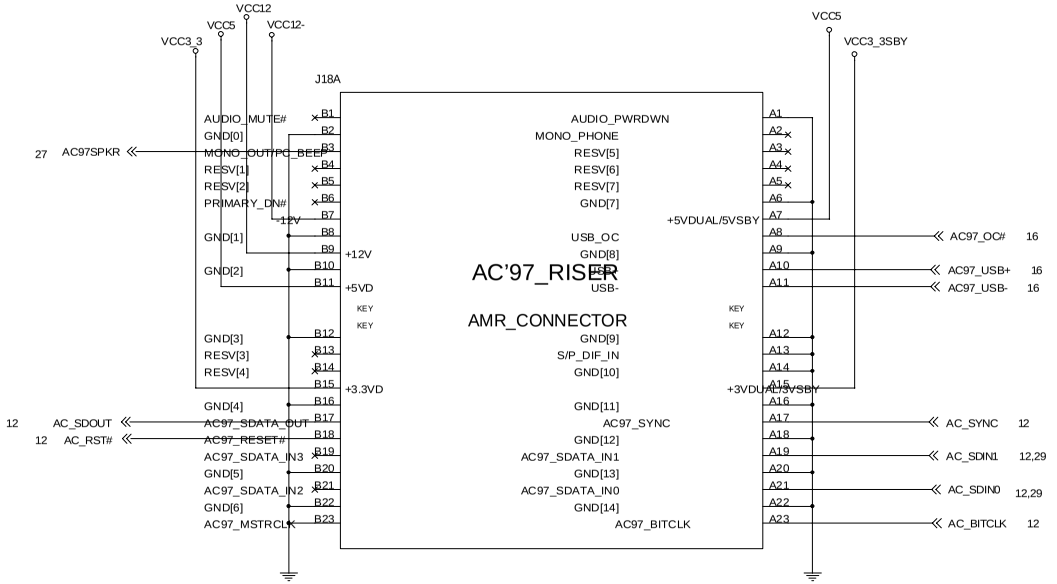


5V to 3.3V Translation / Isolation

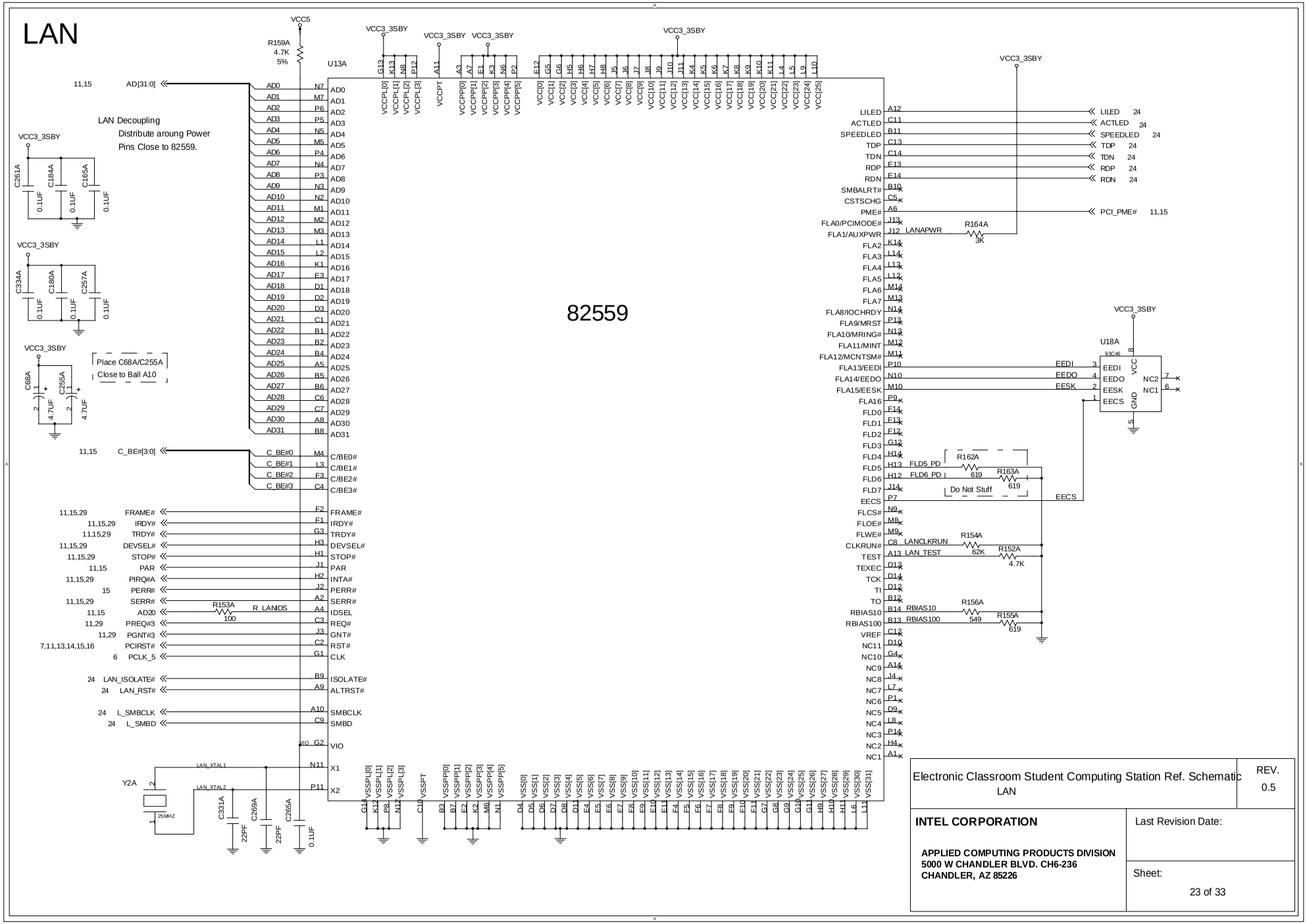


Electronic Classroom Student Computing Station Ref. Schematic VIDEO CONNECTORS	REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 21 of 33

AUDIO RISER



Electronic Classroom Student Computing Station Ref. Schematic AC'97 RISER CONNECTOR	REV. 0.5
INTEL CORPORATION **APPLIED COMPUTING PRODUCTS DIVISION** **5000 W CHANDLER BLVD. CH6-236** **CHANDLER, AZ 85226**	Last Revision Date: Sheet: 22 of 33


LAN
82559
U13A
R159A
4.7K
5%
VCC5
LAN Decoupling
Distribute aroung Power
Pins Close to 82559.
Place C68A/C255A
Close to Ball A10
R153A
100
R_LANIDS
Y2A
25MHZ
LAN_XTAL1
LAN_XTAL2
U18A
93C46
R164A
3K
LANAPWR
R162A
619
R163A
619
Do Not Stuff
R154A
62K
LANCLKRUN
R152A
4.7K
LAN_TEST
R156A
549
RBIAS10
R155A
619
RBIAS100
FLD5_PD
FLD6_PD
Electronic Classroom Student Computing Station Ref. Schematic
LAN
REV.
0.5
INTEL CORPORATION
APPLIED COMPUTING PRODUCTS DIVISION
5000 W CHANDLER BLVD. CH6-236
CHANDLER, AZ 85226
Last Revision Date:
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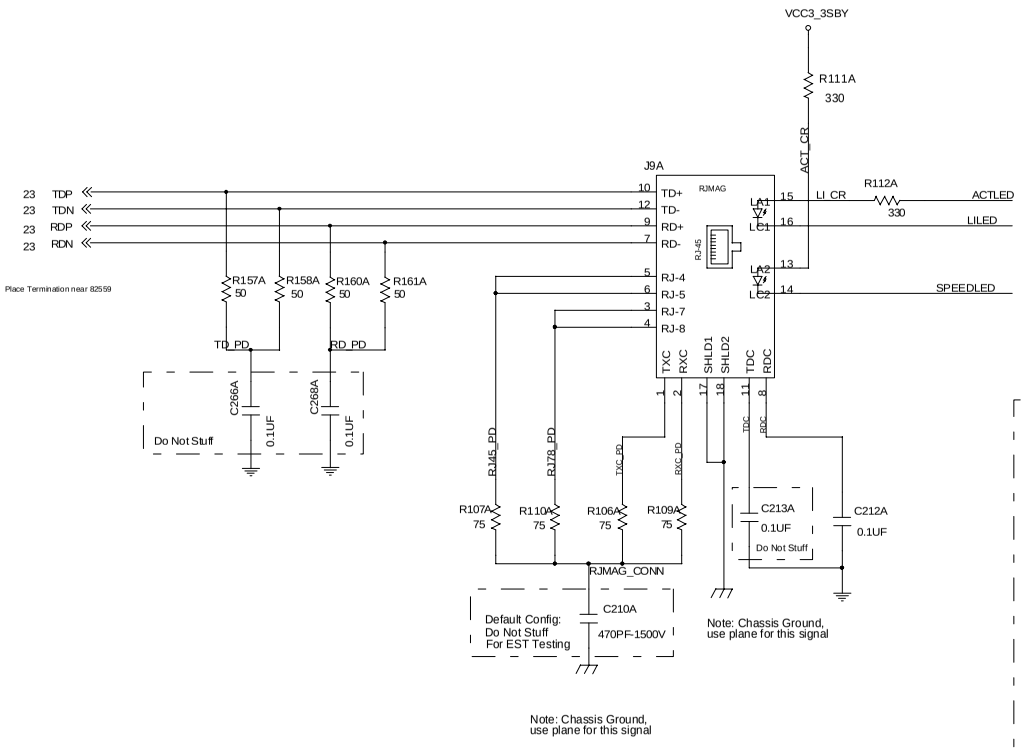
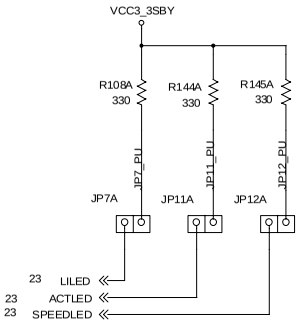
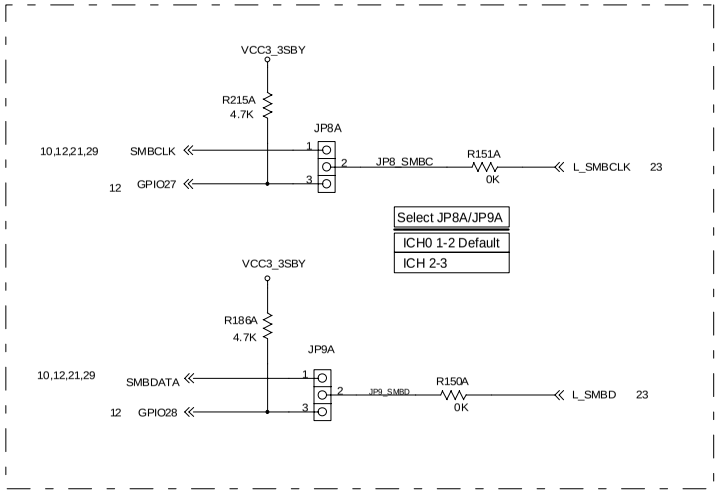
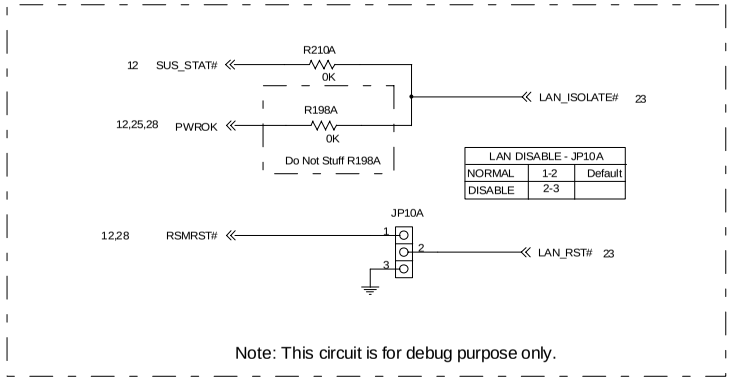
LAN









Electronic Classroom Student Computing Station Ref. Schematic LAN	REV. 0.5
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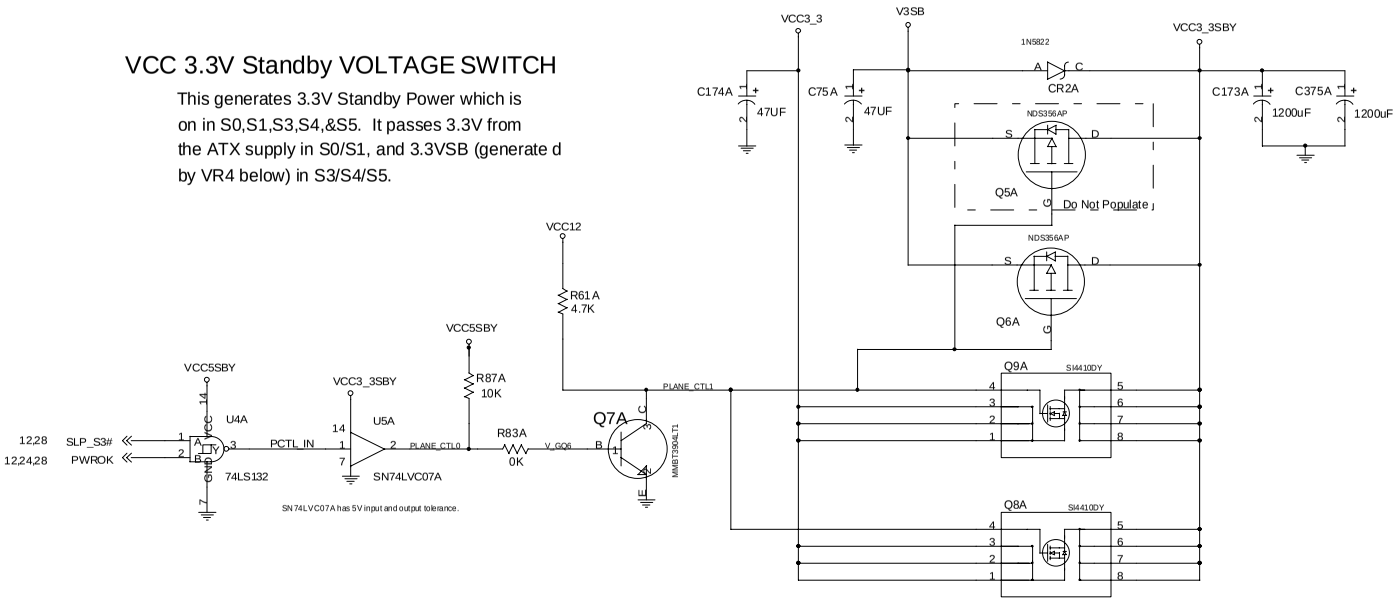
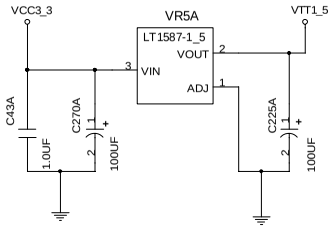
Voltage Regulators

VCC 3.3V Standby VOLTAGE SWITCH

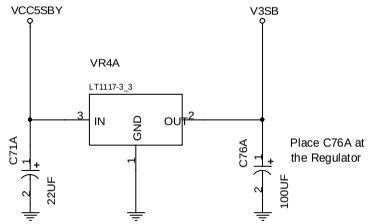
This generates 3.3V Standby Power which is on in S0,S1,S3,S4,&S5. It passes 3.3V from the ATX supply in S0/S1, and 3.3VSB (generate d by VR4 below) in S3/S4/S5.



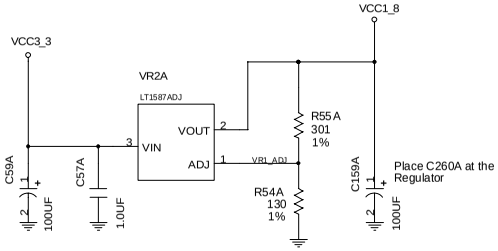
VTT 1.5V VOLTAGE REGULATOR



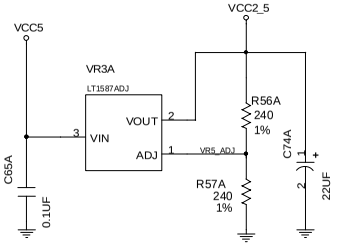
VCC 3.3VSB Regulat or



VCC 1.8 VOLTAGE REGULATOR



VCC 2.5 VOLTAGE REGULATOR



Electronic Classroom Student Computing Station Ref. Schematic VOLTAGE REGULATORS	REV. 0.5
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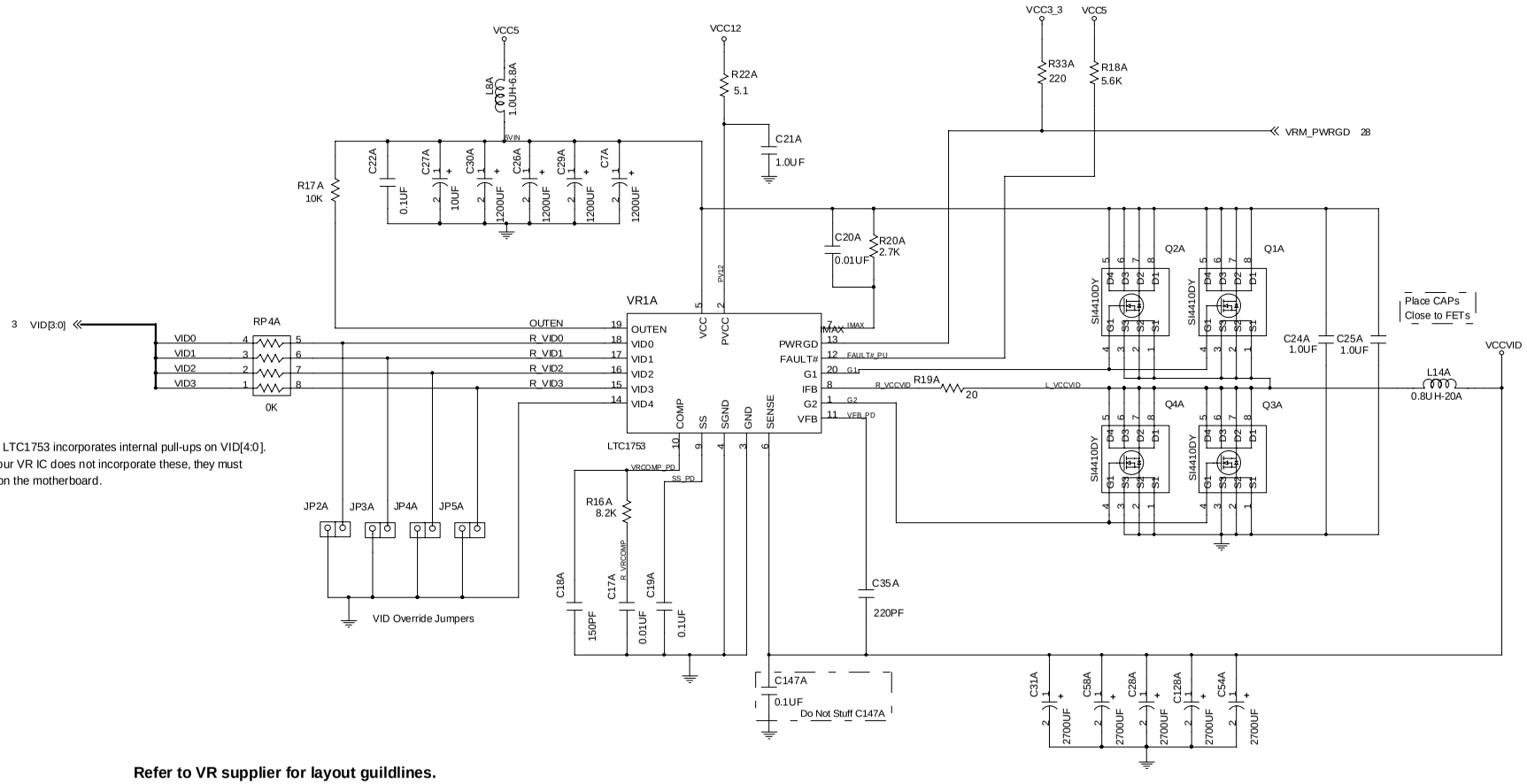
Processor Voltage Regulator



Refer to VR supplier for layout guidlines.

Electronic Classroom Student Computing Station Ref. Schematic VRM 8.4	REV. 0.5
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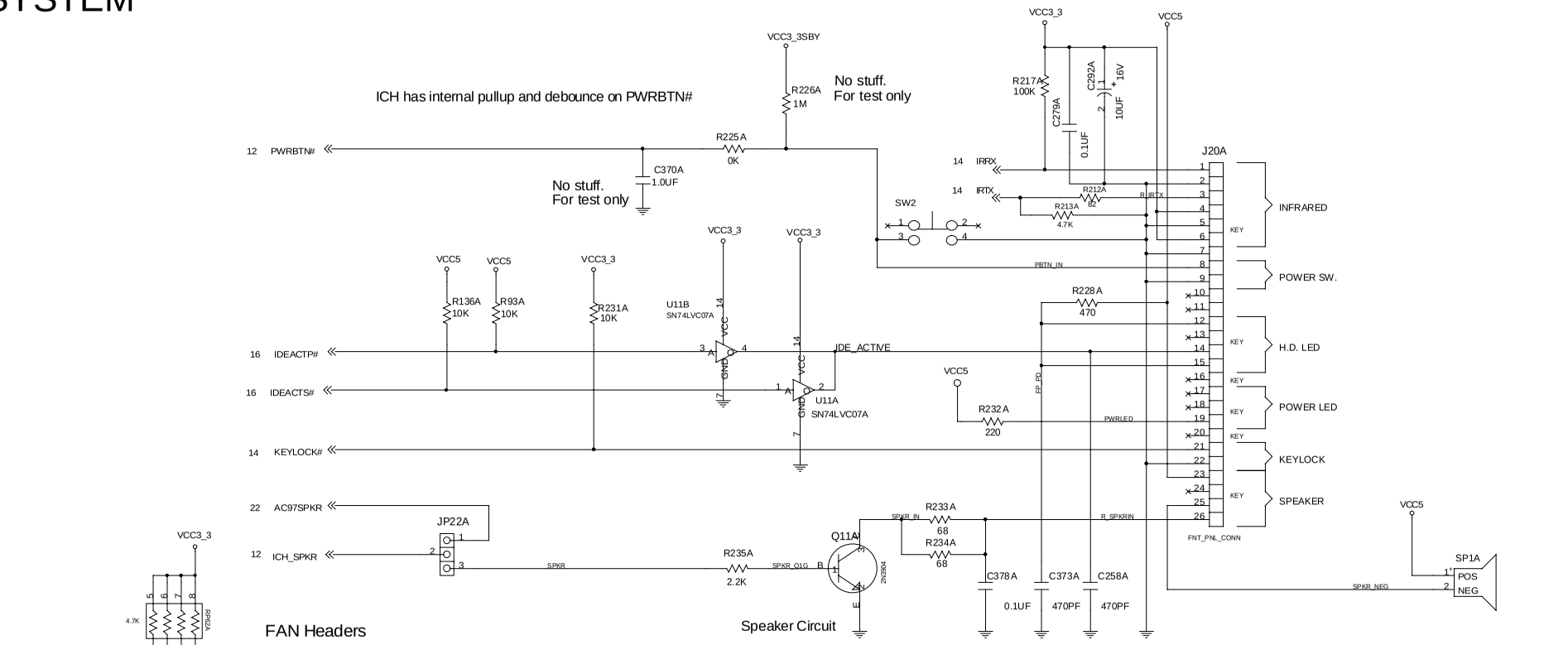
SYSTEM



Electronic Classroom Student Computing Station Ref. Schematic SYSTEM		REV. 0.5
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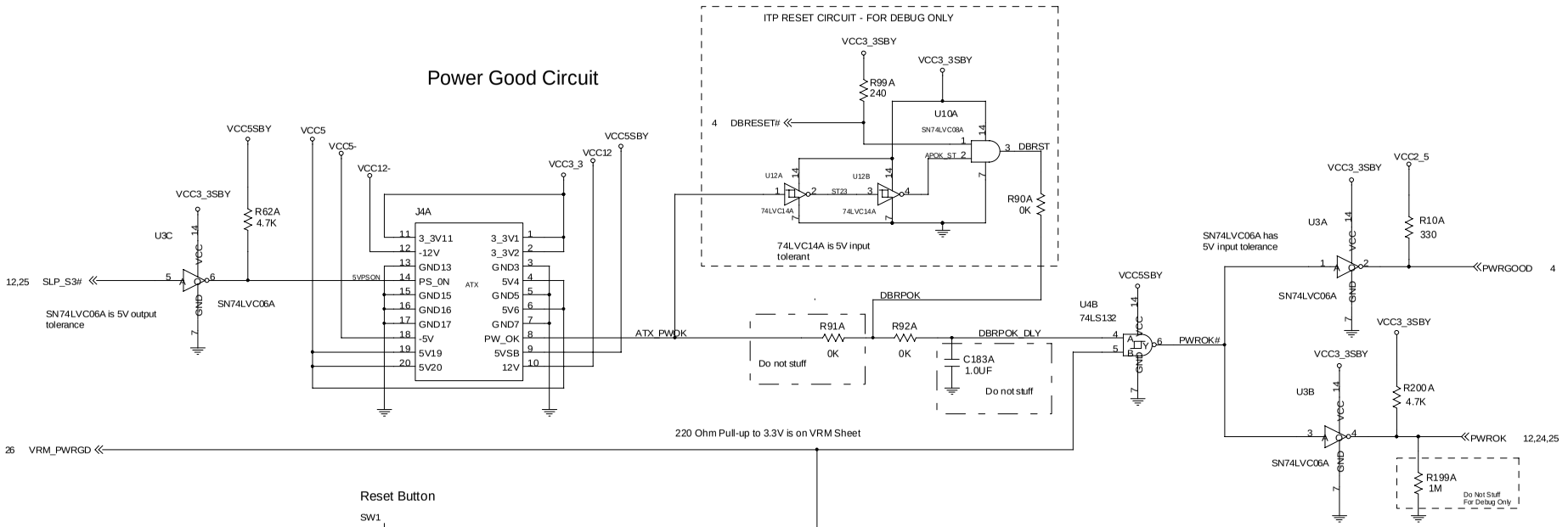
SYSTEM

Power Connector and Reset Control



Electronic Classroom Student Computing Station Ref. Schematic SYSTEM: POWER CONNECTOR AND RESET CONTROL	REV. 0.5
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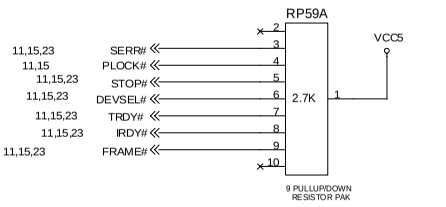
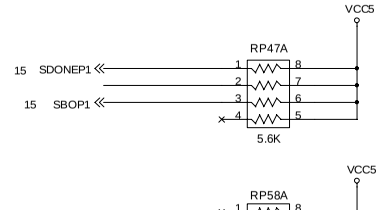
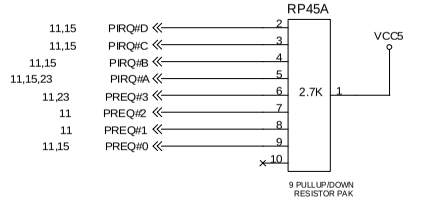
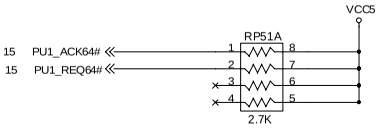
PULL-UP RESISTORS AND UNUSED GATES

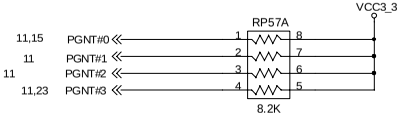
PCI BUS



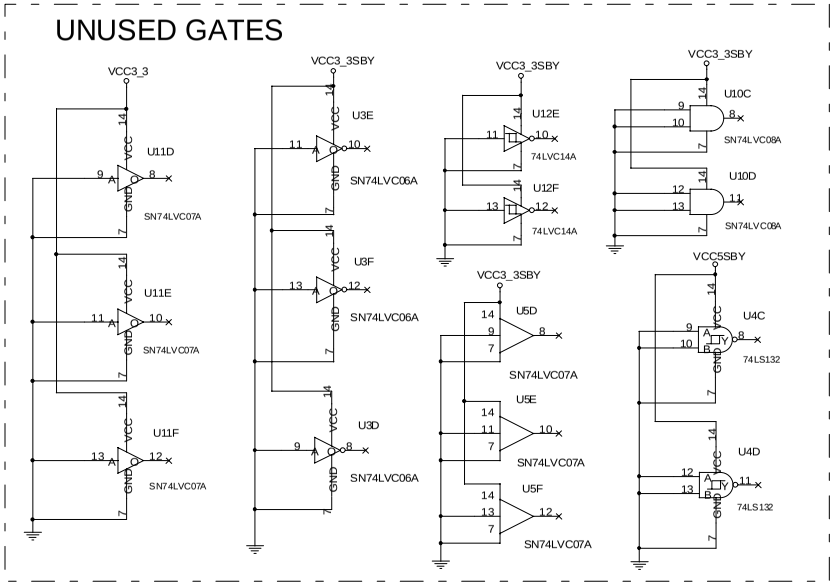




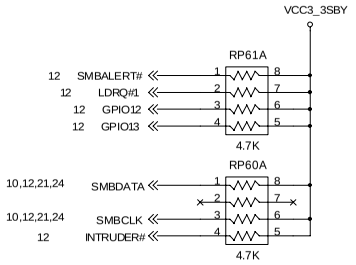


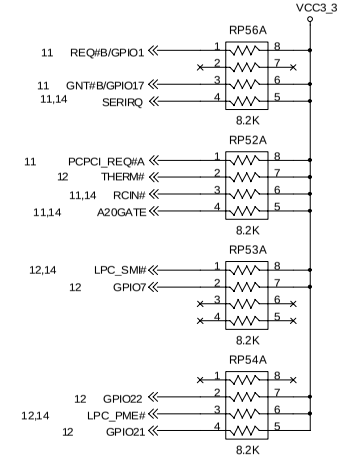


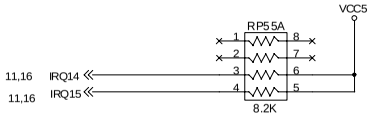
UNUSED GATES

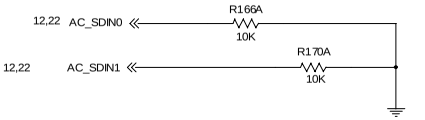


82801AA

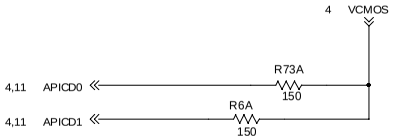


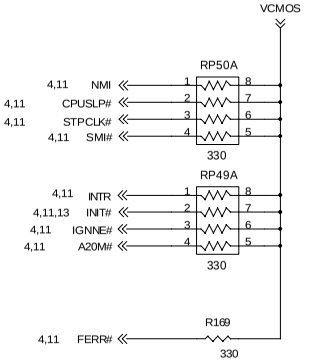


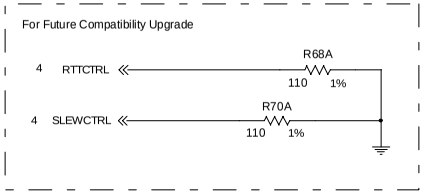




CPU







Electronic Classroom Student Computing Station Ref. Schematic PULL-UP RESISTORS AND UNUSED GATES	REV. 0.5
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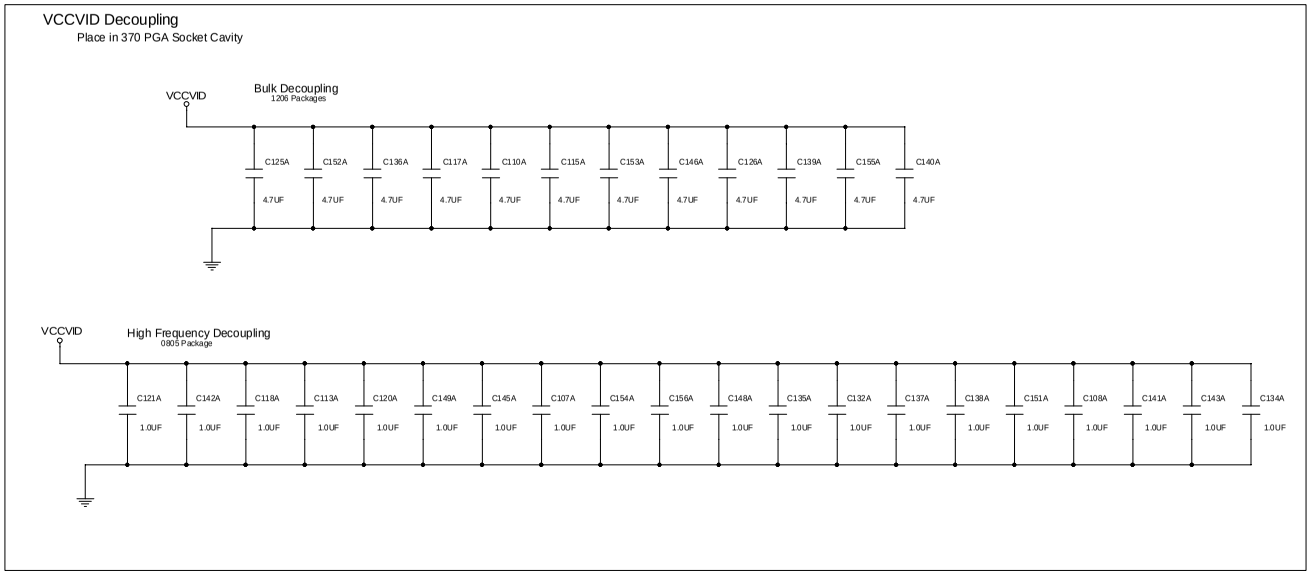
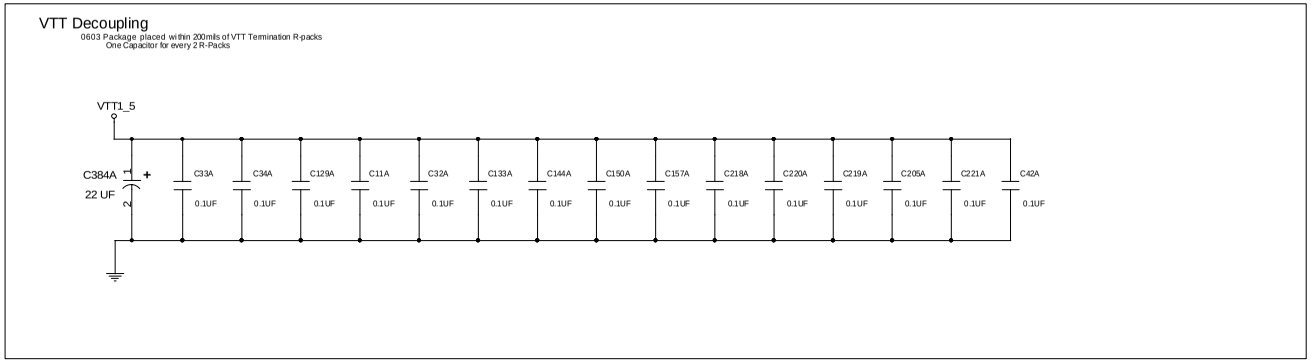
370-pin Socket Decoupling





Electronic Classroom Student Computing Station Ref. Schematic 370-PIN SOCKET DECOUPLING	REV. 0.5
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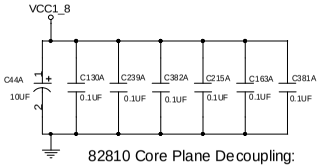
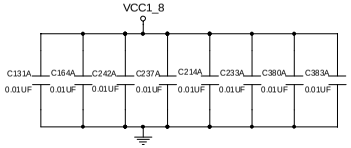
DRAM, CHIPSET, and BULK POWER DECOUPLING

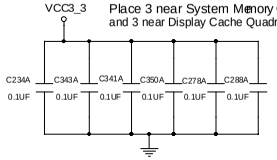
82810 Decoupling



82810 Core Plane Decoupling:
Place 1 .1uF/.01uF pair in each corner, and 2 on opposite sides close to component if they fit.

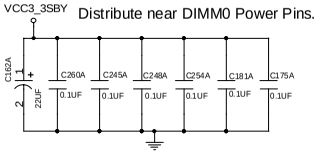


82810 3.3V IO Decoupling:
Place 3 near System Memory Quadrant and 3 near Display Cache Quadrant



System Memory Decoupling

DIMM0 Decoupling:
Distribute near DIMM0 Power Pins.

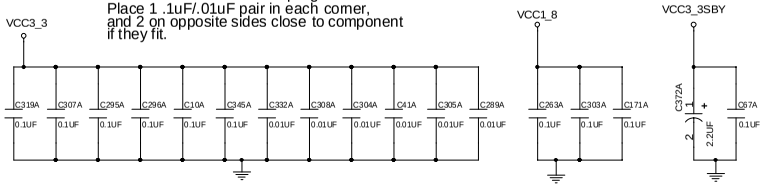


82801AA Decoupling

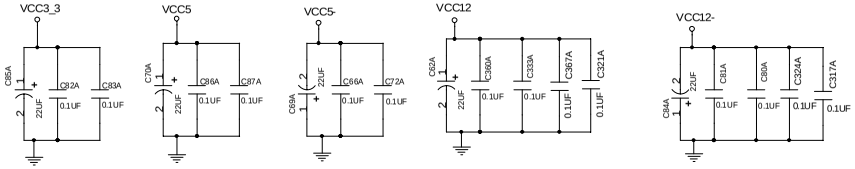
82801AA 3.3V Plane Decoupling:
Place 1 .1uF/.01uF pair in each corner, and 2 on opposite sides close to component if they fit.

Distribute near the 1.8V power pins of the 82801AA

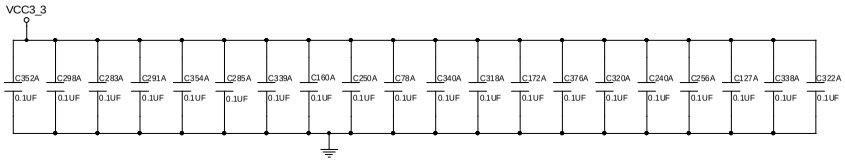
Distribute near the VCCSUS power pins of the 82801AA



Bulk Power Decoupling



3 VOLT Decoupling



Electronic Classroom Student Computing Station Ref. Schematic DRAM, CHIPSET AND BULK POWER DECOUPLING		REV. 0.5
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